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AN EFFICIENT IMPLEMENTATION OF AUTOMATIC WASHING MACHINE CONTROL SYSTEM USING VERILOG

P.USHA [1], CH.KARUNA [2]

1. Assistant Professor, ECE Department, KG Reddy College of Engineering and Technology

2. Assistant Professor, ECE Department, KG Reddy College of Engineering and Technology

ABSTRACT

As described by digital system the language Verilog HDL is widely used in the circuit design, has its own advantages to be able to used as software language which describes hardware features that makes it efficient and has good readability, portability, etc. Its advantages not only reduce the hardware development cycle but also greatly reduce development costs. This article describes the characteristics and application of Verilog HDL and takes the automatic washing machine control system as examples to illustrate the practicality of HDL. The result of simulation shows this method is feasible and effective.

KEYWORDS: *Verilog- Hardware description languages, Automatic washing machine control system.*

1. INTRODUCTION OF VERILOG HDL

With rapid development of science and technology, the design of electronic systems also produce a revolutionary change, a new class of development tools related to electronic systems are spreading quickly. Hardware Description language (HDL) is a method to description of digital circuit. HDL describes a certain function of digital circuit usually has one or more files composition. With the rapid development of electronic system design automation (EDA) and large scale programmable of logic device, HDL has hierarchical description and simulation of any electronic components characteristics, so that the circuit designers and developers could describe the feature of the circuit freely.

Verilog language is a kind of abstract level of hardware description language. This language supports the early abstract design concept, and could realize the later abstract design. It includes the hierarchical structure, which allows designers to describe the complexity of the control.

Verilog HDL is a language which is not only easy to use but also has strong function, especially the Verilog HDL industrial standardization, conforms to the trend of microelectronics technology development. Verilog HDL is used in digital design modeling from the switch level to abstract algorithm design level. These constructions can not only be used to design pattern on hardware inter current behavior, but also on hardware design of scheduling pattern.

2. THE DESIGN OF AUTOMATIC WASHING MACHINE

Because the Verilog HDL has the advantage of powerful language structure and concise code for complex control logic. So, this dissertation is based on Verilog HDL to design the control system of the washing machine.

2.1. The principle of automatic washing machine

All automatic washers, regardless of type, model, or make, have only four basic functions of operation: (1) fill, (2) wash, (3) pump out, and (4) extraction (spin).The important parts of the washing machine; this will also help us understand the working of the washing machine.

a) Water inlet control valve: When you load the clothes in washing machine, this valve gets opened automatically and it closes automatically depending on the total quantity of the water required.

b) Water pump: The water pump circulates water through the washing machine. It works in two directions, re-circulating the water during wash cycle and draining the water during the spin cycle.

c) Tub: There are two types of tubs in the washing machine: inner and outer. The clothes are loaded in the inner tub, where the clothes are washed, rinsed and dried. The inner tub has small holes for draining the water. The external tub covers the inner tub and supports it during various cycles of clothes washing.

d) Agitator or rotating disc: The agitator is located inside the tub of the washing machine. It performs the cleaning operation of the clothes. During the wash cycle the agitator rotates continuously and produces strong rotating currents within the water due to which the clothes also rotate inside the tub.

e) Motor of the washing machine: The motor is coupled to the agitator and produces it rotator motion.

f) Timer: The timer helps setting the wash time for the clothes manually.

g) Drain pipe: The drain pipe enables removing the dirty water from the washing that has been used for the washing purpose.

2.2. Washing Machine Controller specifications

The washing machine controller has the following functionalities:

1. The wash machine has the following consecutive states: idle, fill, wash, drain, fill, rinse, drain, spin.

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2. There is one control line to the washer water feed. Choice of hot or cold water wash is done manually by the user for simplicity.
3. There are two drum rotation speeds: low speed for wash cycle and high speed for the spin cycle. Speed control is accomplished through an electrically controlled mechanism.
4. During the wash cycle, the drum direction of rotation is controlled through the agitator mechanism.

Figure1is the Icon for the washing machine controller indicating main input and output lines

Figure1: Different States of washing machine

The below figure shows the block diagram of the automatic wash machine controller, in which the user selects the start button, the remaining process is continued on the time allocated to each state of the machine i.e. wash, fill, drain etc.

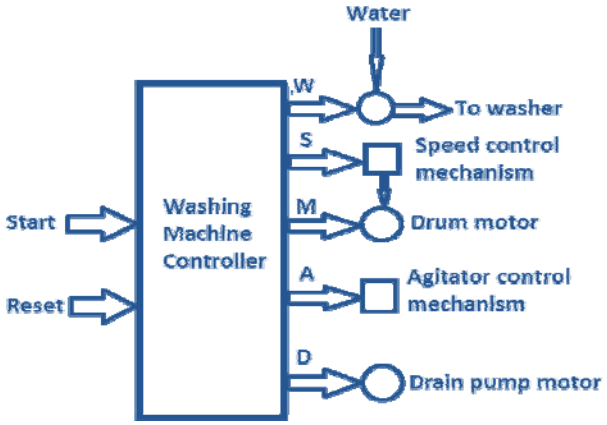

Figure 2: block diagram of washing machine

3. WASH MACHINE CONTROLLER DETAIL

Figure2 shows the main components of the washing machine controller. The controller is composed of two blocks: a finite - sate machine (FSM) block and a timer block. The FSM block receives some signals from the user, from the timer, and from other hardware parts such as the door sensor. FSM block output control the timer block and other hardware components of the washing machine.

Table1 identifies the FSM input and output signals and their functionality. The timer block generates the correct time periods required for each cycle after it has been reset. The timer block is composed of an up-counter and combinational logic to give the correct time signals once certain count values have been achieved. Of course the timer values will be determined by the clock frequency being used in the system. This, however, is beyond the scope of this dissertation.

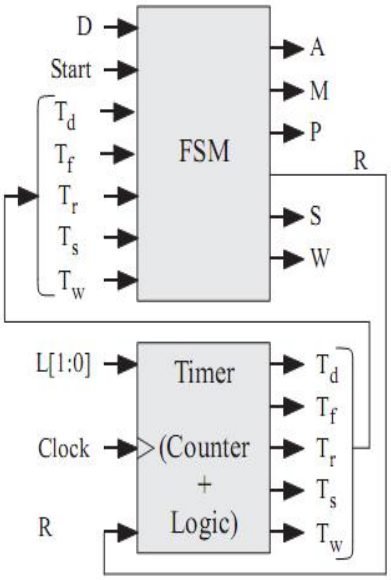

Figure 3: The main components of the washing machine control system.

Table1: Alphabetical listing of input and output signals for the FSM. All signals are active high.

D	IN	Machine door (lid) is open
Start	IN	Start wash machine
T_d	IN	Drain time required to empty the machine tub
T_f	IN	Fill time required to fill the machine tub
T_r	IN	Rinse time
T_s	IN	Spin time
T_w	IN	Wash time
A	OUT	Activate the agitator mechanism
M	OUT	Enable motor
P	OUT	Activate the pump mechanism to drain the water
R	OUT	Timer reset
S	OUT	Activate motor speed control mechanism
W	OUT	Activate water source solenoid

4. PIT FALLS OF ASYNCHRONOUS SIGNALS

The FSM resets the counter each time it starts a new phase (e.g. wash, drain, etc.) in response to the timer outputs. However, for the combination of a Mealy

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machine and an asynchronous counter reset creates problems. When input signal is set it immediately resets the timer before the Mealy machine had a chance to change states. The end result is that the Mealy FSM will be stuck in its present state.This is best illustrated with the detailed timing diagram in Figure3. The present state (PS) of the washer is filling where the drum is being filled with water until the timer asserts the signal T_f. When this condition happens, the FSM must do two actions:

1. Move to the next state Wash

2. Rest the timer

3. Wash clothes until the wash time period Tw is asserted.

We see from the figure that when the reset signal R is asserted, the timer immediately zeros its count and all its output signals are zeroed. This includes the signal T_f. Now we have a problem: The present state of the wash machine is in the fill cycle Fill and the signal T_f is zero. Hence the next state switches back to Fill. The machine will remain stuck in this state and over flow the drum with water. The main problem is that signals like T_f were allowed to change values more than once within the same clock period. This is unacceptable especially for a Mealy FSM. The correct sequence should have been:

Fill → Wash

But now our sequence will be

Fill → Fill

And the machine will never get past the fill phase.

One obvious solution to this problem is to use synchronous reset for the counter. Another solution is to add an extra state after each operation phase of the washer so that checking the time signal and resetting the counter are accomplished in two deferent states.

5. DESIGN FLOW

To design the washing machine the following are required to be done.

1. Design the Mealy state diagram for the washing machine whose specifications are listed in Section2.2.
2. List the states of your state transition diagram
3. Design the timer but having the timing specifications.
4. In new washing machines the door is locked as long as the machine is in operation. Draw the Mealy state diagram that satisfies this requirement.

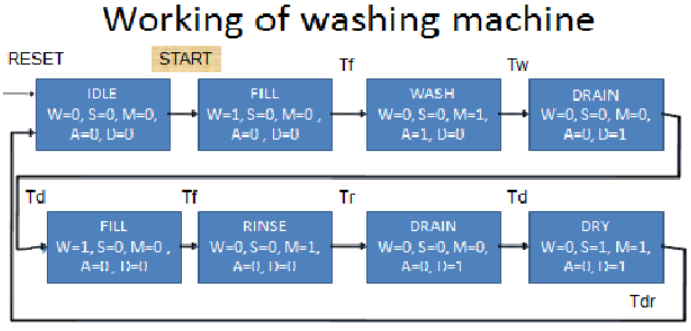

Figure 4: Working of Washing Machine

6. PROJECT REQUIREMENTS

In this project we are required to design, model, and simulate a washing machine controller.

- Use a two or a three-process FSM Verilog coding style for the FSM block.
- Verilog code for the timer design.
- Write a test bench to verify the operation of the timer.
- Synthesize the controller on FPGA and study the performance parameters (delay, FPGA resources, power consumption, and equivalent gate count).

7. PROGRAM

```
module washmachine (rst, clk, start, w, s, a, m, d);

    initial a=0;

        initial m=0;

        initial s=0;

        initial d=0;

 always@ (posedge clk, posedge rst)

begin

    if (rst)

    begin

      state<= _initial;

    end

    else

begin

        case (state)

    _initial:

    Fill:

    Wash:

    Drain:

    Fill:

    Rinse:

    Drain:

    Dry:

    Default:

        endcase

    end

    endmodule
```

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7.1 *Simulation of the Automatic Washing Machine*

When reset signal comes, all of the signals are set to zeros; then if you put on start button the machine will enter water state. As long as you no longer press start button, washing machine will automatically execute the process according to the predetermined process. The simulation results are as shown in figure 4.

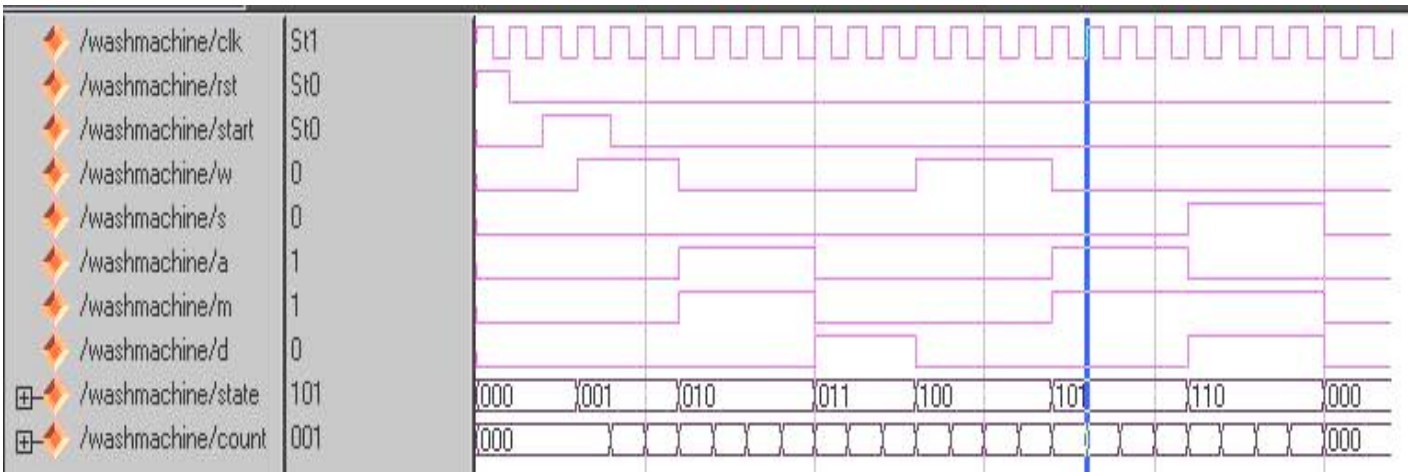

Figure 4.Simulation of Automatic Washing machine controller

8. CONCLUSION

In this paper we use Verilog HDL language to design automatic washing machine control system. We use this powerful language structure and concise code to describe the complex control logic. Through comprehend the corresponding hardware circuit and tools of Verilog HDL language to generate more than traditional logical design method which can adapt to the social development needs. We use hardware description language form digital system design which is not only flexible and convenient but also reduce the cost of development and the development cycle. This design method plays an increasingly important role in the future digital system design.

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