IMPROVED PERFORMANCE OF MEMORY RELIABILITY AGAINST MULTIPLE CELL UPSETS USING HYBRID MATRIX CODE

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ABSTRACT

MCUs (Transient-Multiple Cell Upsets) are getting to be significant issues in the reliability of memories presented to radiation environment. To keep MCUs from bringing about data corruption, more complex ECCs (Error Correction Codes) are generally used to ensure memory, however the fundamental issue is that they would oblige higher delay overhead. As of late, matrix codes (MCS) have been proposed for protection of memory which generally based on hamming codes. Fundamental issue is which they’re double error-correction codes and error-correction capabilities aren’t enhanced in all the cases. Particular paper, novel Hybrid-Matrix-Code (HMC) in light of divide-symbol is proposed to upgrade memory reliability with the lower delay-overhead. Proposed HMC uses decimal algorithm to get the maximum error detection ability. In addition, ERT (Encoder Reuse Technique) is proposed to minimize range overhead of additional circuits without exasperating the entire encoding and decoding procedures. ERT utilizes HMC encoder itself to be a piece of the decoder. The proposed HMC is contrasted with surely understood codes, for example, the current MCS, hamming, and PDS (punctured difference set) codes. They got results demonstrate that mean-time to failure (MTTF) of proposed plan is 452.9%, 154.6%, hamming, MC, and PDS, individually. In the meantime, the delay overhead of the proposed plan is 73.1%, 69.0%, and 26.2% of hamming, separately. The main disadvantage to the proposed plan is which it requires the more redundant-bits for the memory security.

Keywords - ECCS (Error Correction Codes), Decimal Algorithm, MTTF (Mean Time to Failure), Memory, (MCUs) Multiple Cells Upsets.

1. INTRODUCTION

Decimal matrix code is proposed to give improved memory reliability. This methodology utilizes decimal algorithm, which builds the error detection capacity. In proposed work, the encoder is re-used as piece of decoding circuit, in this way lessens the area overhead contrasted with different techniques [1].DMC is proposed to guarantee reliability in the vicinity of MCUs with diminished execution overheads, & 32 bit word is decoded & encoded as a case in light of the proposed techniques.

1.1 FAULT-TOLERANT MEMORY

The proposed schematic of deficiency tolerant memory is delineated. In the first place, amid the encoding (compose) process, bits d are encouraged to the DMC encoder, and after that the level redundant bits h & vertical -redundant Bits v are acquired from the DMC encoder.

1.2 DMC ENCODER

In the proposed DMC, to start with, the partition symbol and mastermind matrix thoughts are performed, that is, n bit word is now separated into k symbols of the m bits (n=k x m), and these symbols are orchestrated in k1 x k2 2D matrix (k= k1 x k2, where the estimations of k1 and k2 speak amounts of lines and segments in the intelligent network individually). Second, the level redundant bits h are delivered by performing decimal number expansion of those symbols per column. Here, every symbol is viewed as a decimal number. Third, the vertical redundant bits v is acquired by double operation among the bits per segment.

To clarify proposed DMC plan. We take a 32-bit word as a sample, as indicated in fig. no. 2. Cells from the d0-d31 are the information bits. Particular 32 bit word has been separated eight-symbols of 4-bit. k1=2 & k2=4 have been picked at the same time.

\[
H_6 H_5 H_4 H_3 = D_3 D_2 D_1 D_0 + D_{10} D_{11} D_{12} D_8 \quad (1)
\]

\[
H_6 H_5 H_4 H_3 = D_3 D_2 D_1 D_0 + D_{10} D_{11} D_{12} D_8 \quad (2)
\]

Furthermore, also for the level redundant bits H19H18H17H16H15 & H14H13H12H11H10, where, “+” sign-speaks to expansion of decimal number.

For vertical-redundant bits v, we’ve

\[
V_0 = D_0 \oplus D_{16} \quad (3)
\]

\[
V_1 = D_1 \oplus D_{17} \quad (4)
\]

Also for the rest vertical redundant bits.

Encoding may be performed by the decimal and paired expansion operations from (1) to (4). The encoder that figures the redundant bits, Bit adders and xor entryways is indicated in fig. 3. In this figure, h19 - h0 are flat redundant bits, v15-v0 are the vertical redundant which are remaining bits u31- u0 are the information bits which are straightforwardly duplicated from d31 to d0. Empower signal En will be clarified in following segment.

1.3 DMC DECODER
To acquire a word being rectified, the decoding procedure is needed. Case in point, to begin with, got redundant bits with $h_4h_3h_2h_1h_0$ and $v_3 - v_0$ are produced by the got information bits $d$ second, the flat disorder bits $h_4h_3h_2h_1h_0$ and vertical-disorder bits $s_3 - s_0$ can be computed as takes after,

$$\Delta h_4h_3h_2h_1h_0 = h_4h_3h_2h_1h_0' - h_4h_3h_2h_1h_0$$  \hspace{1cm} (5)

$$S_0 = V_0 \oplus Y_0$$  \hspace{1cm} (6)

What’s more, likewise for the rest vertical disorder bits, where “-” speaks to decimal whole number subtraction

In the proposed DMC decoder is portrayed which is comprised of the accompanying sub modules, and each executes a particular assignment in decoding procedure: disorder adding machine, error-corrector and error-locator. It may be seen from this assume that redundant-bits must be then recomputed from got information bits $d$ and contrasted with the first set of redundant bits keeping in mind the end goal to acquire the disorder bits $\Delta h$ and $s$. At that point error locator utilizes $\Delta h$ and $s$ to recognize and find which bits a few errors happen in. At last, in error corrector, particular errors may be adjusted by inverting the estimations of error bits.

In the proposed plan, the circuit territory of DMC is then minimized by the reusing its encoder. Particular is known as the ERT. The ERT can lessen the territory overhead of DMC without irritating the entire encoding and decoding procedures. From fig. 4, it can be watched that the DMC encoder is reused for acquiring the disorder bits in DMC decoder. Accordingly, the entire circuit zone of DMC can be minimized as an after-effect of utilizing the existent circuits of encoder. In addition, this figure additionally demonstrates the proposed decoder with an empower signal en for choosing whether the encoder should be a piece of the decoder [3].

**1.4 POINTS OF CONFINEMENT OF SIMPLE BINARY ERROR DETECTION**

For the proposed twofold error detection technique in [13], in spite of the fact that it obliges low redundant bits, its error detection capacity constrained. The primary purpose behind this is that its error detection instrument is in light of parallel.

We show the points of confinement of this basic twofold error detection [13] utilizing a straightforward sample. Give us a chance to assume that bits $b_3, b_2, b_1, b_0$ are unique information bits and the bits $c_0$ and $c_1$ are redundant bits indicated in fig. The bits $c_0$ and $c_1$ are acquired utilizing the paired algorithm.

$$D_{0\text{correct}} = D_0 \oplus S_0.$$  \hspace{1cm} (7)
Fig. No. 5: Advantage of Decimal-Error-Detection using algorithm H4H3H2H1H0

Fig. No. 6: Types of MCUs can be revised by our proposed DMC.

These outcomes mean that error bits b2 and b0 are wrongly viewed as the first bits so that these two error bits are not amended. This case shows that for this basic twofold operation [13], the quantity of even bit errors can’t be identified.

1.5 POINT OF PREFERENCE OF DECIMAL ERROR DETECTION

In the past examination, it has been demonstrated that error detection [13] in light of parallel algorithm can just distinguish a limited number errors. Nonetheless, when the decimal algorithm is utilized to distinguish errors, these errors can be identified so that the decoding error can be kept away from. The reason is that the operation system of decimal algorithm is not the same as that of double. The detection strategy of decimal error detection utilizing the proposed structure demonstrated as a part of fig. 2 is completely portrayed. As a matter of the even redundant bits h4h3h2h1h0 are from the original information bits in the symbol 0&1 according to (1)

\[ H_4H_3H_2H_1H_0 = D_1D_0D_9D_8 + D_3D_2D_1D_0 \]

At that point, the level disorder bits \( \Delta h_4h_3h_2h_1h_0 \) can be acquired utilizing decimal whole number subtraction

\[ \Delta H_4H_3H_2H_1H_0 = H_4H_3H_2H_1H_0 - H_4H_3H_2H_1H_0 = 0110 - 1001 = 0010. \]  

The decimal estimation of \( \Delta h_4h_3h_2h_1h_0 \) is not "0," which speaks to that errors are identified and situated in symbol 0 or symbol 2. In this way, the exact area of bits which were flipped may be situated by utilizing the vertical disorder bits s3 - s0 and s11 - s8. At long last, every these errors can be remedied by (7). Subsequently, in view of decimal algorithm, the proposed technique has higher resistance capacity for memory against MCUs.

Fig. No. 7: Error-type can be corrected by proposed DMC

(1) The decimal number of information bits in symbols, 0 and 2 is equivalent to \( 2^{m-1} \).

(2) All the bits in symbols 0 and 2 are upset

Expecting that these two elements have been accomplished, by encoding and procedures of DMC, h4h3h2h1h & h4h3h2h1h0 are then figured, as it takes after

At this point when MCUs happen in symbol-0 & symbol-2, that is, bits in symbol-0 are upset to ‘1’ from the ‘1100’ (d3d2d1d0=1111) and the bits in symbol 2 are to "0111" from "0110" (d11d10d9d8=0111) amid the decoding process, got even redundant bits h4h3h2h1h are then figured initially, as it takes after:

This outcome means that no errors happen in symbols 0 and 2 and memory will endure a failure. Be that as it may, this case

Case in point, when \( m = 4 \), the likelihood of decoding,
\[ P_{\Delta H=0} = 4 \times \left( \frac{1}{2} \right)^r \times P_{MCU8} \approx 0.001 \]  \hspace{1cm} (20)

If \( m = 8 \)

\[ P_{\Delta H=0} = 4 \times \left( \frac{1}{2} \right)^r \times P_{MCU16} \approx 0.000001 \]  \hspace{1cm} (21)

\( P_{MCU8} \) speaks to the likelihood of eight upsets in a given word, and comparatively for \( P_{MCU16} \). In addition, as per the radiation analyzes in and [18], it can be acquired that the word in a memory as a rule has a predetermined number of successive errors and the interim of these errors not more than three bits. In this way, this ought not to be an issue.

### 1.6 DEPENDABILITY AND OVERHEADS ANALYSIS

In this segment, the proposed DMC has been actualized in hdl, mimicked with modelsim and tried for usefulness by given different inputs. The encoder and decoder have been blended by the synopsys design compiler in the smic 0.18 æm technology.

### 1.7 FAULT/FLAW INJECTION

The correction coverage of PDS [9], MC [15], hamming, and the proposed DMC codes are gotten from one million examinations.

### 1.8 UNWAVERING QUALITY ESTIMATION

The reliability of our proposed code can be dissected as far as the mean time to failure (MTTF). It is expected that MCUs touch base at memories taking after a Poisson distribution [19]. For single word, the correctable likelihood \( r(s) \) after \( s \) radiation occasions can be given

\[ R(s) = \sum_{i+j+z \leq S} P_i^1 P_j^2 \cdots P_z^y \]  \hspace{1cm} (22)

Where, \( t \) is the maximum number of errors and \( P_z \) is the correctable likelihood upon the gathering of radiation occasion \( S \) which causes \( Z \) errors.

For a memory with \( m \) words, the correctable likelihood \( j(s) \) after \( s \) radiation occasions can be given by,

\[ J(s) = \sum_{a+b+\cdots+e=s} \frac{C_a^b M^1 R_a^1 R_b^2 \cdots R_e^y}{M^x} \]  \hspace{1cm} (23)

Where, \( x \) (x less than equal to \( S \)) is the quantity of words influenced by radiation occasions, \( C_n^k \) is the choice of \( x \) from \( m \) words in memory, and \( R_a^1 \) speaks to the correctable likelihood when \( e \) radiation occasions influence \( x \) words.

In the event that we expect that the word number \( m \) is 32 and the correctable likelihood \( P_s z \) can be gotten from table i, the probabilities \( j(s) \) of distinctive protection codes have been demonstrated in fig. 9. It can be seen that the correctable likelihood \( j(s) \) of proposed plan is bigger than different codes.

At that point the MTTF can be given by (24), which is function of integral (23)

\[ \text{MTTF} = \int_0^\infty J(t)dt. \]  \hspace{1cm} (24)

Table ii shows MTTFs of distinctive codes for diverse occasion entry rate \( ? \). In this table, we can see that the proposed plan has higher MTTF by than 122.6%, 154.6%, and 452.9% contrasted with PDS [9].

When all is said in done cases, for the proposed technique, it can be gathered that the bigger the word widths, the higher the resilience capacities and the better the reliabilities. For instance, for a 64-bit word, when \( k = 2 \times 4 \) and \( m = 8 \) the correction capacity of to 9

For a 128-bit word, when \( k = 2 \times 4 \) and \( m = 16 \), the correction capacity of the proposed technique is up to 17 bits. In capacities of PDS, MC, and hamming are littler than DMCs under the same word widths.

### 1.9 OVERHEADS ANALYSIS

The delay overhead of DMC is 26.2%, 69.0%, and 73.1% of PDS [9], shows that the memory with the proposed plan performs quicker than different codes. Distinctive decoding algorithms could bring about diverse overheads. The decoding algorithm of PDS[9] is more complex than that of different codes; therefore, it has maximum zone, power, and delay overheads.

\[ \beta = \frac{\text{Redundant bits}}{\text{Redundant bits} + \text{Information bits}}. \]  \hspace{1cm} (25)

In the event that the estimation of \( \beta \) is little, the code needs lower memory cell overheads. From this table, we can see that hamming code has the slightest \( \beta \) esteem however its correction ability is a consistent (1).

In 90-nm technology, more than three errors have been seen in radiation test [1], [2], [17], and PDS are bad decisions for ensuring memory. The proposed plan needs higher \( \beta \) esteem than different codes yet it has higher correction ability.

Subsequently, creators ought to pick the ideal mix of \( k \) and \( m \) taking into account the radiation test to give a decent exchange off in the middle of reliability and redundant bits. we have likewise utilized a metric to evaluate the effectiveness of our proposed plan contrasted with PDS, MC, and hamming, which is called correction coverage per cost (ccc) and can be figured as take after [15]:

\[ \text{CCC} = \frac{\text{Correction Coverage}}{\text{Cost}} \]  \hspace{1cm} (26)

Where cost is acquired by

\[ \text{Cost} = \text{Area} \cdot \text{Power} \cdot \text{Delay} \cdot \text{Redundant bits}. \]  \hspace{1cm} (27)

Demonstrates the estimations of this metric for distinctive security codes. From this figure, we can see that the proposed plan has a CCC quality than other codes except that stand out MCU happens. Along these lines, taking into account the outcomes in Table lii and fig. 10, proposed plan is very suitable for rapid memory.
applications. It ought to be specified that when the quantity of errors is more than two for every word, hamming and MC [15] codes can’t redress any errors.

Fig. No. 8 : (a) Proposed fault tolerant CAM utilizing decimal-error-detection (b) 32 bit words organization in a CAM (k=1×4 & m=8).

2. PROBLEM STATEMENT

2.1 DELAY REPORT FOR EXISTING DESIGN

2.2 SLICES, LUT, FLIP FLOPS FOR EXISTING DESIGN

Number of Slices: 180 out of 3584 5%
Number of Slice Flip Flops: 32 out of 7168 0%
Number of 4 input LUTs: 312 out of 7168 4%
Number of bonded IOBs: 107 out of 141 75%
Number of BRAMs: 6 out of 8 75%
Number of GCLKs: 1 out of 8 12%

2.3 OUTPUT WAVEFORM

In the existing design the last 5 output bits are not changing. These values are changing for the next time of run. In the starting dec_en is 0 and ram_en is 1. As the image is showing the last five values are not changing. In the second round dec_en is 1 and ram_en is 0. Then the output is coming correct.
3. RESULTS

3.1 SLICES, LUT, FLIP FLOPS FOR EXISTING DESIGN

Number of Slices: 136 out of 3584 (3%)
Number of Slice Flip Flops: 32 out of 7168 (0%)
Number of 4 input LUTs: 256 out of 7168 (3%)
Number of bonded IOBs: 107 out of 141 (75%)
Number of BRAMs: 6 out of 8 (75%)
Number of GCLKs: 1 out of 8 (12%)

3.2 DELAY OF PROPOSED DESIGN

3.3 OUTPUT WAVEFORM FOR PROPOSED DESIGN
4. CONCLUSION

HMC was proposed to guarantee the reliability of the memory. Proposed protection-code used decimal algorithm to recognize errors, so that more errors were distinguished and remedied. Got results demonstrated that the proposed plan has a predominant protection level against extensive MCUs in memory. Additionally, the proposed decimal error detection technique is an appealing assessment to distinguish MCUs in cam in light of the fact that it can be consolidated with bics to give a satisfactory level of resistance. The main downside of proposed HMC is which more number of redundant-bits are obliged to keep up higher reliability of memory, so that a sensible mix of k and m ought to be decided to expand memory reliability and minimize the quantity of redundant bits taking into account radiation analyzes in real execution. In this manner, future work will be directed for the decrease of the redundant bits and the upkeep of the reliability of the proposed technique.

REFERENCES


