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A LOW POWER DUAL MODULUS PRESCALER

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ABSTRACT

Bipolar technologies do offer a high range of frequency of operation but at the expense of power consumption. So, to minimize the power is of prime importance. The prescaler block do consists of various sub modules which comprises of nMOS and pMOS. These transistors can be effectively used so as to reduce the area as well as the power consumption. The D Flip-Flop internal circuit is also shown here along with the waveform and the power consumption has been brought to 5.4 µW. Compared with these, the prescaler fabricated in CMOS processes usually operate at lower frequencies. The highest reported operating frequency for CMOS prescaler is 15 GHz. The circuit has been fabricated in a 130 nm technology and consumes relatively high power (115mW). Extra feedback networks were used to increase the operating frequency to 14 GHz in a 0.18 µm CMOS process. A phase shifting prescaler switches among signals with varying phases to achieve two or more divide ratios. The highest operating frequency for phase shifting prescaleris 13 GHz and consumes 41 mW of power. A Dual Modulus Prescaler is one of the complicated building blocks in phase lock loop. The 90 nm technology will have the pull-up and pull-down pMOS and nMOS so that the signal strength does not become weak which forms the input to the AND gate for the extra clock pulse to get added i.e. 1 pulse at the output is produced. This report presents a low voltage, low power, Dual Modulus Prescaler. The circuit is to be fabricated in a 90 nm CMOS process and voltage required is 1.2 V. This forms the main voltage that is given to the circuit.

Index Terms: *— CMOS Prescaler, Microwind, Phase Lock Loop, D-flip flop.*

1. INTRODUCTION

1.1 SCOPE

Microelectronics is one of the most important industries in the world. Almost every consumer product contains one or more electronics system. From cellular phones and digital video to modern automobiles, all of these contain electronically controlled and/or programmable parts. Considering these facts, it is not a surprise to know about the tremendous growth of the electronics industry since the past decade. Today, the trend is developing whole Systems on a Chip (SOC), that is integrate all the electronic system's functions, including digital and analog circuits, on a single silicon die.

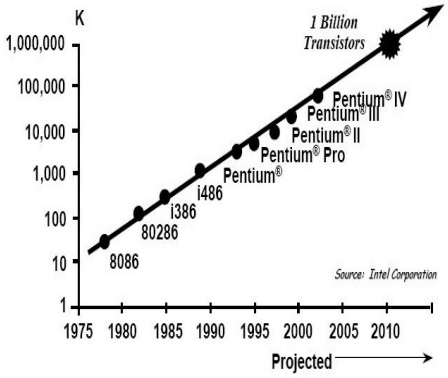

Figure 1: Moore's Law

1.2 MOORE'S LAW

According to Moore's law, "Silicon technologies will double the number of transistors per chip in every 18 months" [1]. As per this statement technology is at express highway & tremendous value for chip technology. Chip manufacturing technology is suddenly on the threshold of a major evolution. Increased demand for newer devices like mobile phones & hand held computers along with the high performance PCs is pushing the chip manufacturing companies to not only shrink the chips in size but also boost the performance as shown in figure 1.2. Due to this reduction in the size of the chip, the power consumption is drastically reduced & also the size of the chip reduces. This facilitates to lower the design area.

1.3 CHIP TECHNOLOGY

It leads to the development of greatest illustrations of chip technology and it is beyond imagination that how small these chips are: "The human red blood cell is only 7 µm big and yet today's technologies could fit around 400 transistors on the surface of the cell. Circuit lines of these chips are 1000 times thinner than a human hair." The credit goes to today's CMOS chip technology [2]. The trend of CMOS technology improvement continues to be driven by the need to integrate more functions into a given area of silicon. The evolution of important parameters such as IC complexity, gate length, switching delay, and supply voltage with a perspective vision down to the 22 nm CMOS technology. Every day new products go out to the market offering less power consumption, reduced size, all together with additional functions and capabilities. By one side, it is important to consider that

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CMOS technologies have played an important role in this development of the integrated applications. The design of a Very Large Scale Integration (VLSI) chip - one containing 100,000 or more transistors - is a fundamentally hierarchical process that begins with a general idea of what the chip is supposed to do. Designers must then describe the functional modules that will result in a piece of hardware able to perform the specified functions unlike most everyday devices whose inputs and operations are effectively predefined, VLSI chips must be able to react to a constantly changing environment. Levels of design abstraction initializes from behavioral level where basic simulation of design performed.

2. METHODOLOGY

2.1 BLOCK DIAGRAM

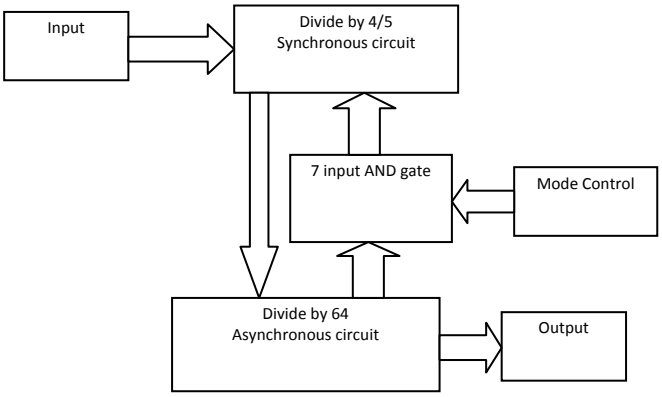

Figure 2: Block Diagram

Basically a prescaler is a circuit which generates an output signal related to an input signal by a fractional scale factor [7]. Prescaler circuits are useful in many applications such as clock generation in digital circuits and phase-locked loop (PLL) circuits. It is usually desired to divide a clock signal by an integer N. Prescalers are used in the feedback loop between the output of a voltage-controlled oscillator (VCO) and the phase frequency detector in phase locked loop frequency synthesizers to generate higher frequencies. A typical known prescaler is arranged to divide either at an M factor or at an (M+1) factor. A prescaler has two available divide ratios and has an input control line that allows a control circuit to set a first mode where the prescaler divides by a first divide ratio, or set a second mode where the prescaler divides by a second divide ratio. This terminology of divide by ratio greatly facilitates in the mobile communication where the carrier needs to be removed and only the information signal has to be considered. Also, this has the role in the modulation and the demodulation techniques also.

2.2 DESCRIPTION OF DUAL MODULUS PRESCALER

i) Block diagram of Dual Modulus Prescaler consist of

1. Divide by 4/5 synchronous circuit.

2. Divide by 64 asynchronous circuits.

3. Seven (7) input AND gate.

4. Mode Control (MC).

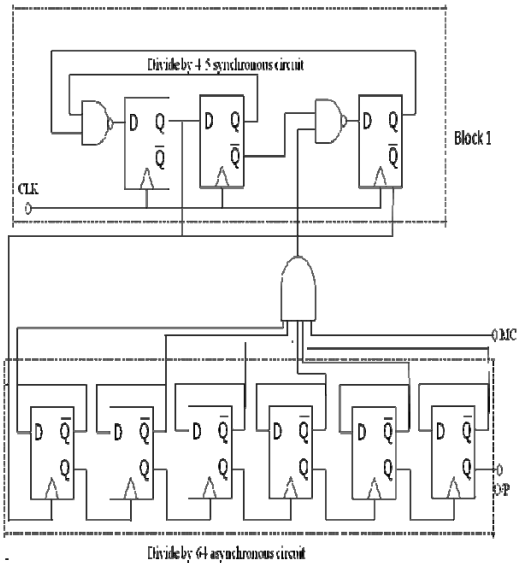

Figure 3: Functional Diagram of Dual Modulus Prescaler

Nano-CMOS Based Low Power Dual Modulus Prescaler. As dual-modulus prescaler consists of a synchronous divide-by-4/5 circuit and an asynchronous divide-by-64 circuit as shown in figure 3.1. The total divide ratio is 256 and 257 when the modulus control, MC is set to low and high respectively. Output is taken from last stage of divide by 64 asynchronous circuits.

ii) Divide by 4/5 synchronous counter (Block 1)

In this prescaler, the synchronous divide-by-4/5 circuit **is** the most critical part because it operates at the highest frequency. The divide-by-4/5 circuit consists of three differential D-flip-flops and 2 NAND gates to implement the modulus selection. The first two flip-flops are connected as a divide-by-4 circuit while the third flip-flop adds an extra clock period delay for the divide-by-5 operation. Both the flip-flops and NAND gates are in the critical path. To reduce the propagation delay, the NAND gate and flip flop are merged together. To better balance the delays, the output of first flip-flop is chosen to drive the asynchronous divider.

iii) Divide by 64 asynchronous counter (Block 2)

It is a chain of divide by 2 asynchronous counters. In the Sequential Logic the D-type Flip-Flop work and they can be connected together to form a Data Latch. Another useful feature of the D-type Flip-Flop is as a binary divider, for Frequency Division or as a "divide-by-2" counter. Here, the inverted output terminal Q (NOT-Q) is connected directly back to the Data input terminal D giving the device "feedback" as shown below.

iv) Divide by 64

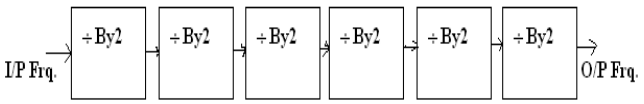

Figure 3.3: Divide By 64

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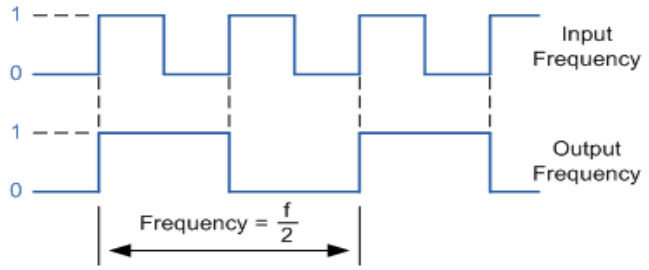

Figure 4: Output of D flip flop as Divider

It can be seen from the frequency waveforms above, that by "feeding back" the output from NOT Q to the input terminal D, the output pulses at Q have a frequency that are exactly one half of the input clock frequency [10]. In other words the circuit produces frequency division by factor of 2.

v) Equivalent CMOS Inverter

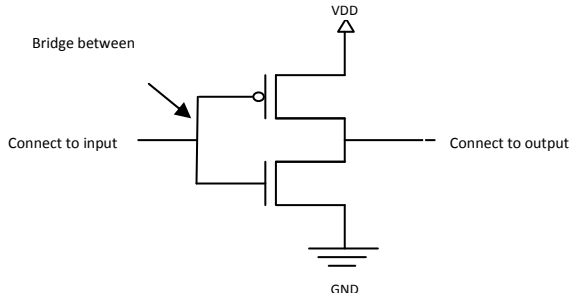

Figure 5: Inverter

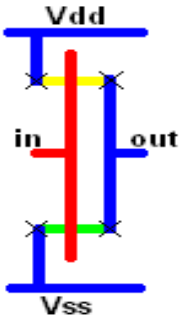

Figure 3.6: Stick Diagram of Inverter

The above two diagrams reflects the actual circuit and the layout for the same. While the different colour combination of the Figure 3.6 reflects the red colour as the polysilicon, Yellow indicates p diffusion, Green indicates the n diffusion and the blue colour indicates the metallic contacts to connect the Vdd and Vss. Thus, ensuring full connectivity to the n MOS and the p MOS transistors. This combination of the two transistors forms the Inverter.

3. RESULTS

Table 1: Transistor requirement

Sr. no.	Module	D Flip-Flop required		Total gate count	
		Traditional design	Proposed design	Traditional design	My design
1.	4/5 divider	3	3	60	36
2.	Divide by 64	6	6	120	72
TOTAL		9	9	**180**	**108**

Table 2: Analysis for the gates required per D Flip-Flop

Sr. no.	Type or Design	Gates used	Transistors used per gate	Total count per D Flip-Flop
1.	Traditional D Flip-Flop	5	4	20
2.	SCL	--	16	16
3.	nMOS & Inverters	4 inverters and 4 NMOS	02	12

Table 3: Entire sub module analysis for gates required in my design

Sr. no.	Sub module	Devices used	nMOS	pMOS	Total count
1.	4/5 divider	3 D Flip-Flop & 2 NAND gates	24+4	12+4	12*03= 36 04*02=08
2.	7 input AND gate	---	7	7	07*02= 14
3.	Divide by 64 unit	6 D Flip-Flop	48	24	12*06= 72
TOTAL					130

Table 4: Entire sub module analysis for gates required in SCL (previous design)

Sr. no.	Sub module	Devices used	nMOS	pMOS	Total count
1.	4/5 divider	3 D Flip-Flop & 2 NAND gates	16+2	02	16*03= 48 04*02=08

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2.	7 input AND gate	---	7	7	07*02= 14
3.	Divide by 64 unit	6 D Flip-Flop	16	--	16*06= 96
TOTAL					166

Gross percentage decrease in the gate count=

(Gate count in the previous design - Gate count in my design) / (Gate count in the previous design)

= [(166-130)/ 166] * 100 = [36/166] * 100

=0.2168 * 100 = 21.68 %

3.1 Fan-out

Low state fan-out= I_{OL}/ I_{IL} = 0.02/0/001= 20

3.2 Propagation Delay

$T_{pHL}= 0.69\times R_nC_L$

$T_{pLH} = 0.69\times R_pC_L$

3.3 Figure of Merit

Figure of Merit for the design = P.D * P_D

= 6.095 ns * 335 μW = 2.0418 * 10^{-12} = 2.0418 pJ

4. CONCLUSION

A Dual Modulus Prescaler is one of the complicated building blocks in phase lock loop. The 90 nm technology have the pull-up and pull-down pMOS and nMOS so that the signal strength does not become weak which forms the input to the AND gate for the extra clock pulse to get added i.e. 1 pulse at the output is produced. This report presents a low voltage, low power, Dual Modulus Prescaler. The circuit is fabricated in a 90 nm CMOS process and voltage required is 1.2 V. This forms the main voltage that is given to the circuit.

Thus, the implementation of the Dual Modulus Prescaler has been carried out with the least power consumption up to 334.995 μW. The voltage required was 1.2 V and the current required is up to 279.162 μA. Here, the overall area of the chip has been reduced by 21.68 % and is found to be 23.58 μm x 10.5 μm.

This all has been done because of the use of D Flip-Flop by using only NMOS and inverters. Therefore the overall transistors required per D flip flop were 12 as compared to the traditional D Flip Flop which consisted of 20 transistors per D Flip Flop. It has drastically reduced the number of components on chip.

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BIOGRAPHIES

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