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Correction of Power Factor by Single Inductor Three-Level Bridgeless Boost Converter

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Abstract

Single inductor three-level bridgeless boost power factor correction boost converter is proposed with a natural voltage clamp & that can be treated in series by applying the two boost converter. In this paper proposed converter can be charged & discharged in the different boost sub –circuits. For slow down the operation two diodes is used as for the converter operating performance, in alter of the used rectifier diodes. It has a high utilization factor in one circuit with having the one inductor.

Introduction

Electricity is the backbone of the economy and development of any country and for a quality electricity or power a suitable power factor is very essential for the supply of electricity in this report we have discussed on every point of power factor and its correction by the soft switching method over the conventional method of power factor correction. We have discussed about the single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp. This method is based on the soft switching & switched mode power supply (SMPS).

Correction of Power Factor by Single Inductor Three-Level Bridgeless Boost Converter having Voltage Clamp Property

This type of converter has very high output efficiency due to the soft switching technique and to give the further detail of the circuit we will have to discuss about soft switching.

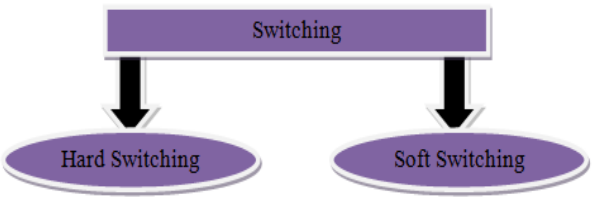

Figure 1: These are mainly two types of switching

Hard Switching

Hard switching are the conventional switching which is heavy, complex, costly & larger in size as well as it has some drawbacks of loss of electrical power & lower output efficiency because it consumes as well as stores some power which affects the output electrical efficiency. And these draw backs gives birth to the concept of soft switching.

Soft Switching

To overcome the drawbacks of hard switching, soft switching technique is introduced. In this type of switching semi-conductor power electronics switches are used. In this concept two types of switching is done.

(a). Zero voltage switching

(b). Zero current switching

Zero Current Switching

In zero current switching IGBT is used in which when current becomes at zero value then the circuit gets switched of and by this type of turn off method there is no loss in electrical power and by hence its efficiency is enhanced.

Zero Voltage Switching

In zero voltage switching the MOSFET is used as a power electronic switch in which switch voltage is brought to zero volt gate pulse is applied in gate terminal of switch after that smooth turn ON is achieved with eliminated switching loss.

Three Level Single Inductor Bridgeless Boost PFC with Voltage Clamp Property

Earlier the dual boost power factor correction rectifier is a good topology with full utilization of two MOSFET but its drawback is high conduction noise.

After that the totem pole boost bridgeless power factor rectifier is introduced with lower conduction mode (CM) noise but some drawback of reverse recovery characteristics of MOSFET don't gives it continues current mode (CCM) operation. To remove its draw back a new bridgeless power factor correction with two boost converter circuit replacing the switch leg is used to replaced the conduction of MOSFET body diode and it can also operate in continues current mode (CCM) but in this circuit a floating gate driver with extra inductor is required which makes it heavier.

After that a bidirectional boost bridge less power factor correction rectifier is introduced with bidirectional switches. But it also suffers from conductionmode (CM) noise.To replace all these demerits and drawbacks the single inductor with three-level bridgeless boost PFC rectifier is introduced. inthis converter two slow diode are working as rectifier diode as well as clamping diode simultaneously. The slow diode and the intrinsic diode of MOSFET operates with switching frequency and replace the problem of reverse recovery, nature voltage clamp has achieved and voltage stress of the devices becomes half of the output voltage.

Advantages of the Converter

(a). Only one inductor is required.

(b). Low device voltage stress with the nature voltage clamp.

(c). Voltage stress low and reduction of conduction losses and low CM noise interference.

(d). Utilization factor of the semi conductor device becomes high.

Operational Analysis

To solve the problem remain in the three level bridgeless boost power factor correction with only one inductor is proposed in this given circuit. Its description is given in the figure below.

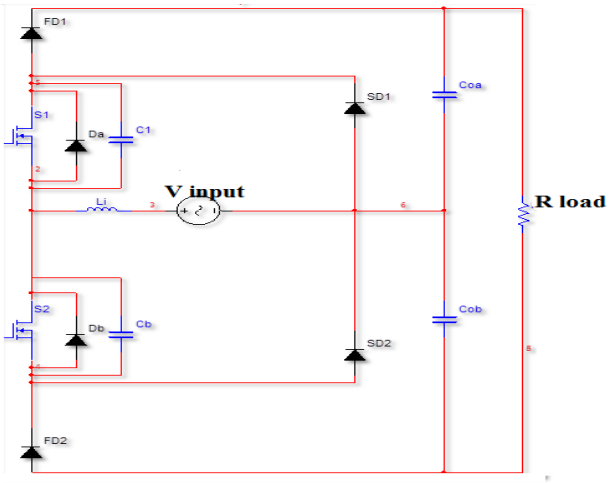

Figure 2: Proposed converter

The proposed topology needs only one inductor and their device utilization factor is very high. In this circuit two slow diodes (S_{D1}& S_{D2}) can be used as rectifier diode as well as voltage clamping diode simultaneously. By this nature voltage clamping can be achieved. Two output capacitors (C_{0a}& C_{0b}) are also connected in the circuit to clamp the line output to reduce the conduction mode noise. And by this the total output voltage becomes high due to the series output structure. And it can be used for inverter or uninterrupted power supplies. In this circuit two MOSFET are used as switch (S_1&S_2) this two MOSFET are connected with two intrinsic diode (D_a&D_b) and two junction capacitors (J_{c1} & J_{c2}), F_{D1} & F_{D2} are the fast diode & L_i is the input inductors connected to the MOSFETs , R_0 is the load resistance $V_i(t)$ is the line input & V_{0a}& V_{0b} are the output voltages (V_{0a} = V_{0b} = V_0).

The proposed converter circuit can be used as two separate boost converter circuit for each output signal during half time cycle. To make circuit simple all the devices are assumed to be ideal. The output capacitor are kept so large so that the voltage in output are remains constant.

Modes and Stages of the Proposed Converter Circuit

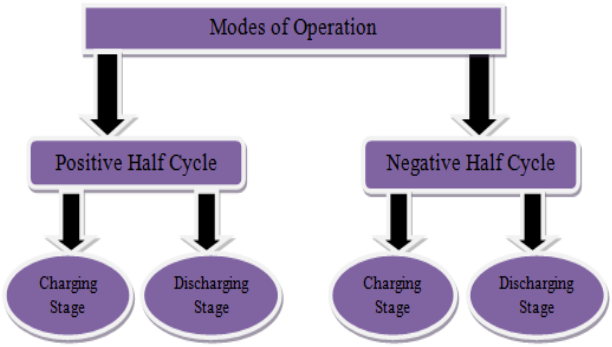

Figure 3: Modes and stages of operation

Charging Stage of Positive Half Cycle

During charging stage of positive half cycle the circuit works between t_a to t_b switch S_2 turns on at t_a the current is commutated from F_{D1} and D_a to S_2 and S_{d2} .as F_{D1}& D_a are connected in series and reverse recovery of F_{D1} and D_a are dominated by F_{D1} (fast diode) and hence the F_{D1} blocks the whole voltage of reverse recovery and D_a is still forward biased without current. When $S_2$is fully on then the voltage across the F_{D1} is clamped to V_{0a} by D_a ,$S_2$and S_{D2}.

Discharging Stage of Positive Half Cycle

During discharging stage t_b to t_c , at $t_b$$S_2$ turns off, the current is shifted from S_2& $S_{D2}$to F_{D1} and D_a . $S_2$and S_{D2} are in series &S_2 is a MOSFET there is no issue of reverse recovery theoretically for the slow diode. In next section it will be further explained as the result when the S_2 is fully off , $S_{D2}$is still on without current & the voltage across the S_2 is clamped to V_{0a} by S_{D2} , D_a& F_{D1} .

In this stage the inductor L_i current is discharged & also decreases linearly. The capacitor C_{0a} is charged up and the capacitor C_{0b} is still delivers the power to load since S_{D2} is forward biased and F_{D1} and D_a are in the ON state, so that the voltage across S_{D1}, S_2 and F_{D2} are $V_{0a,}$ V_{0a}, & V_{0b} respectively.

Charging Stage of Negative Half Cycle

During charging stage the period between t_d to t_e. S_1 turn on at t_d .the current commutated from F_{D2} and $D_b$to S_1 &S_{D1}.$F_{D2}$and D_b are connected in series the reverse recovery of F_{D2} and D_b are dominated by the fast diode F_{D2} . Thus F_{D1} blocks the whole reverse voltage &D_b is still forward biased without current. When S_1 is fully ON the voltage across F_{D2} is clamped to V_{0b} by D_b, S_1&S_{D1} .

During this stage the inductor (L_i) current charged by input voltage $V_i(t)$ and increases linearly . the capacitor C_{0a} and C_{0b} delivers the power to the load in series. D_b is forward biased and S_1 and S_{D1} are in ON state. So, the voltage across F_{D2} , s_{D2} and F_{D1} are V_{0b}, 0 and V_{0a} respectively .this stage stops working when the switch S_1 turns of at t_e.

These are the descriptive explanation of the charging mode in the negative half cycle in which the inductor of the power factor correction circuit based on the boost converter is working in the charging mode. And the discharging mode will be discussed just next after this charging mode.

Discharging Mode of Negative Half Cycle

During discharging stage if negative half cycle the period is from t_e to t_f .att$_e$$S_1$ turns off . The current is shifted from S_1 and S_{D1} to F_{D2} and D_b. As S_1 and S_{D1} are in series &S_{1S} is a MOSFET.

There is no reverse recovery voltage for slow diode theoretically. It will explain in the next part. as a result when S_1 is fully off , S_{D1} is still ON with no current & the voltage across the S_1 clamped to V_{0b} by S_{D1} , D_b& F_{D2}. In this stage the inductor L_i current is discharged and decreases linearly. The capacitor C_{0b} is charged up and the capacitor C_{0a} still delivers power to the load. S_{D1} is forward biased and F_{D2} and D_b are in the ON state. So the voltage across S_{D2} ,S_1 and F_{D1} are V_{0b} , V_{0b} , and V_{0a} this mode ends when S_1 turns ON at t_f again.

Design Consideration

The proposed converter can be treated as continues current mode (CCM), discontinuous current mode (DCM) and current resonance mode(CRM), and the operation is similar to the traditional single switch converter.

The output capacitor is charged up throughout half cycle and discharged by the load current in the left over half cycle. so the charge current I_{chg} and the discharged current I_{dischd} through each capacitor in a line cycle are given below.

$$I_{chg} = I_0 - 2I_0 \cos(2\pi f_L t) \quad (1)$$

$$I_{dischd} = -I_0 \quad (2)$$

Where f_L is the line frequency and I_0 is the DC output current.

Based on the above equation the RMS current for the each capacitors are given in the next equation which is double then that in the conventional boost power factor correction converter. It is reasonable due to the series output structure.

$$I_{CRMS} = \sqrt{2} I_0 \quad (3)$$

Based on the capacitor discharge and charge current given in the equation (1), the voltage ripple for the output capacitor C_0 can be introduce as

$$\Delta V_C = I_0 \frac{1}{2\pi f_L C_0} \left(\frac{\sqrt{3}}{2} + \frac{2\pi}{6}\right) \quad (4)$$

Peak to peak output ripple voltage is the addition of the two capacitors (voltage ripple) which is given in the next equation it is double than that in a traditional boost PFC converter

$$V_r = 2I_0 \frac{1}{2\pi f_L C_0} \quad (5)$$

The output capacitance can be designed based on the required voltage ripple given in equation (5) and its RMS current is given in (3).

Simulation and Its Result

The simulation is done in the SIMULINK, a part of the software called MATLAB.

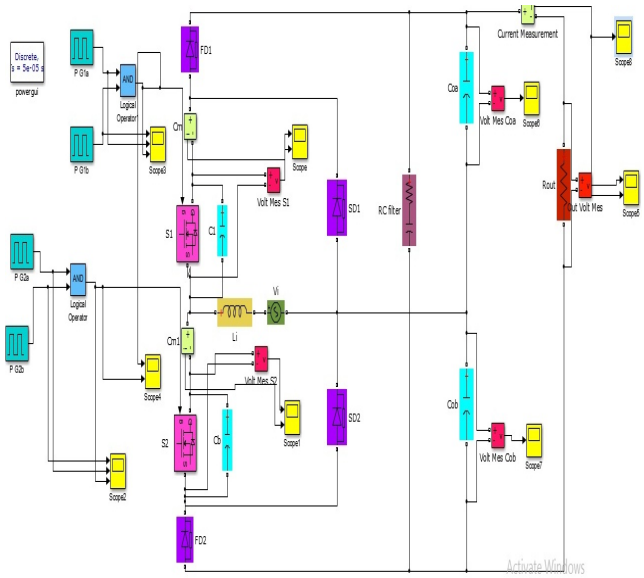

Figure 4: Equivalent circuit of proposed topology in SIMULINK

Figure 4 is the equivalent simulated proposed topology, in which two fast diodes (F_{D1} and F_{D2}) and two slow diodes (S_{D1} and S_{D2}) are connected to the circuit because of their different work on different timings. The reverse recovery of the slow diode is very slow and the properties of voltage clamping makes it important in the circuit where as the fast diode has very high reverse recovery characteristics, two MOSFET is used in the circuit as the main switch naming S_1 and S_2. Capacitors are used for delivering the power to the load in series. Inductor is used in the circuit for charging and discharging purposes.

All above component is simulated in the manner discussed previously and the output of the simulated circuit will obtain. All the components are of the same parameter which is discussed in the different tables of chapter no. 4 in which the detailed description of the given component is discussed.

Now we will discuss on the different parameter of the component used in the simulated circuit.

Table 1: Components and their parameter for simulate the proposed circuit.

SYMBOL	PARAMETER	SPECIFICATION
$V_i(t)$	Line input	240v RMS, 796v DC, 1000w, 1.25A
V_{0a}/V_{0b}	DC buses	400VDC ±5%
V	Total output voltage	800VDC
P	Full output power	1000W
$F_{switching}$	Switching frequency	100kHz
S1,S2	MOSFET	SPW47N60C3
F_{D1},F_{D2}	Fast diode	IDH12SG60C
S_{D1},S_{D2}	Slow diode	KBPC3510
L_i	Input inductor	700mH
C_{0a},C_{0b}	Output capacitor	2μF

Wave Forms across the Switches

Input Gate Pulse Waveform of the Switch S_1

The output wave form of the auxiliary switch is given below which is operating in the positive half cycle.

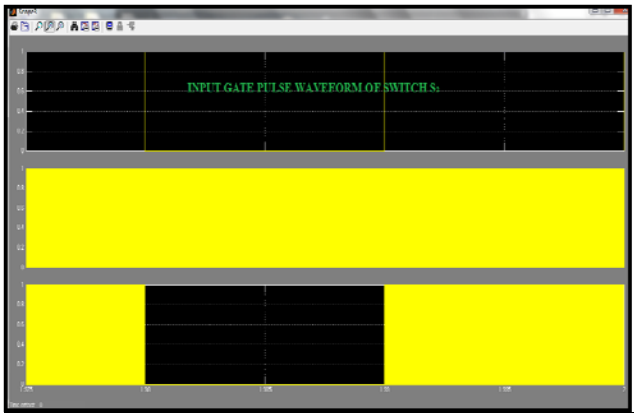

Figure 5: The input gate pulse waveform of the switch S_1.

In case of the first auxiliary switch S_1, it working in the positive half cycle and since it is connected through the AND gate hence it gives the out when both the pulse generator gives the pulse otherwise no output will obtain. Because it operates through the AND gate and the output of the AND gate will obtain in the condition only when both the input is positive or one. Now we will discuss about the output wave form of the second auxiliary switch S_2.

Output Waveforms (Current & Voltage)

Waveform Switch S_1

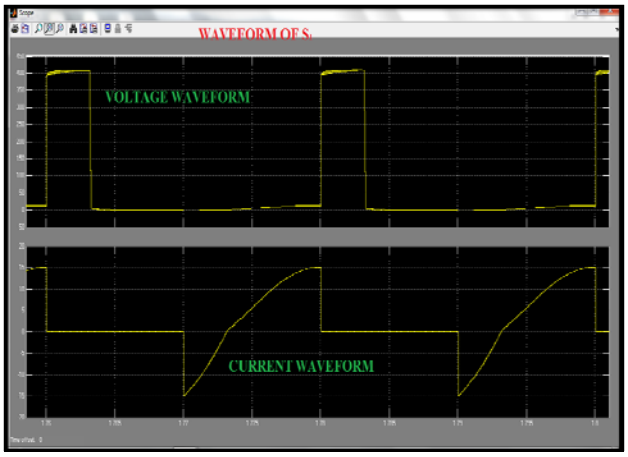

Figure 6: Output waveform of switch S_1

In the above figure of output waveform which is obtained from the switch S_1 we have seen that when the current is at the minimum (i.e zero) the value of the voltage is at its maximum Value and this is the condition satisfy the zero voltage switching (ZVS) where the value of the voltage becomes maximum after when the value of the current becomes zero and after that when the current is going to be increasing the value of the voltage drops drastically and becomes zero , at instant when the current attains its maximum value as shown in the wave form at the same instant it becomes and the voltage attains its maximum value and this condition satisfy the zero current switching (ZCS).

Waveform of Switch S_2

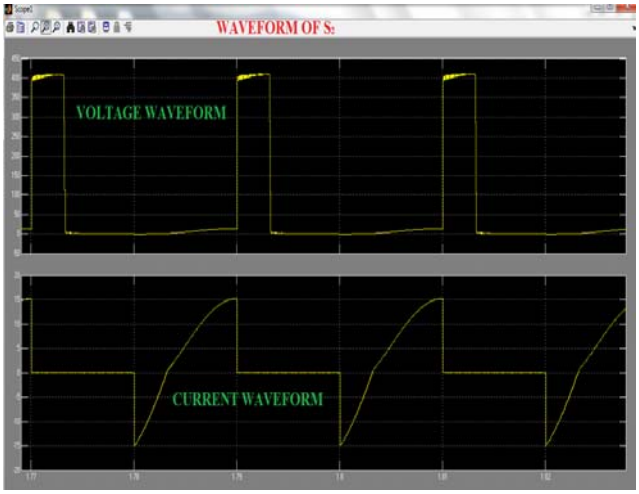

Figure 7: Output waveform of switch S_2

Output Load Waveform

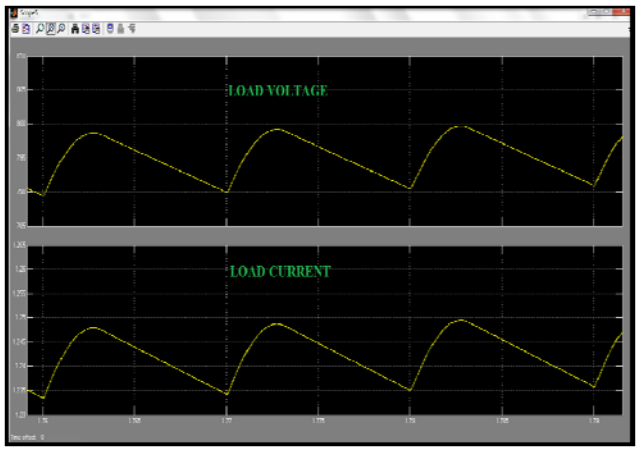

Figure 8: Load voltage and current waveform

The waveform of load current and load voltage is shown in this above figure we have seen that when the two voltage signal of 400V each passed through the LC filter then the combined waveform of both the input signal comes from the output capacitor is

obtained of 800V and the main thing we have seen is that both the current and the voltage signal are in the same manner., I.e unity power factor or the corrected power factor which gives ideal quality power supply which is good for the uninterrupted power supply or for the battery charging which will give the longer life. And by this we have achieve the main goal of PFC for quality power.

Conclusion

A single inductor three-level boost bridgeless power factor correction rectifier with nature voltage clamp characteristics has proposed in this thesis work.

In the proposed converter circuit two slow diodes are used as clamping diode and rectifier diode simultaneously. Though the slow diode and the intrinsic diode of the MOSFET operates with the switching frequency. So the problem of the reverse recovery has short out. The voltage stress of all the power electronic devices is reduced to ½ of the total output. With achievement of nature voltage clamping.

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