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Economic Full Adder Circuit in VLSI Using Shannon Expansion

[1]M. Singh, [2]M. K. Pandit, [3]A. K. Jana

Abstract

This paper presents an efficient high-speed 8-bit full adder using Shannon's expansion. The adder is designed and implemented using 180nm CMOS process technology. The proposed adder provides a good compromise between cost and performance in carry propagation adder design. The proposed full adders for low power and high performance neural network training circuits has been implemented using Shannon decomposition based technique for sum and carry operation. The hardware includes multiplier circuit for product term and an adder circuit to perform summation. The proposed full adder is designed using tanner EDA tools and the resulting parameters such as 25% improvement in power dissipation and 22% improvement in transistor count from the simulated output when compared with ripple carry adder cell. It decreases the computational time compared to ripple carry adder and thus increases the speed.

Keywords: Shannon theorem, Shannon Expansion, Adder Cell, Propagation Delay, Transistor count.

Introduction

Arithmetic functions such as addition and multiplication have a special significance in VLSI designs. Most of the applications require these basic operations, but good performance has been a challenge in silicon implementation. Adders are the fundamental circuit in all the arithmetic designs. With advances in technology, we need adders having high speed, low power consumption, regularity of layout and hence the less area or even a combination of them in one application, the growing demands of communication adder.

An adder or summer is a digital circuit that performs addition of numbers. Many computers and processors use adders in the arithmetic logic units. Although adders can be constructed for many numerical representations such as binary coded decimal or excess-3 the most common adders operate on binary numbers.

Binary adders are the most essential logic elements within a digital system and also helpful in units other than Arithmetic units (ALU), such as multipliers, dividers, memory addressing. Therefore the binary addition essential that any improvement in binary addition can result in a performance boost for any computing system and help improve the performance of the entire system.

By using Karnaugh map method the expression forum and carry. This paper discusses about adder cells using Shannon's expression are given as styles and comparing the performance in terms of power dissipation, delay and area.

Figure 1: Block diagram of Full Adder

Table 1: Truth Table of Full Adder

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum(S) = A xor B xor Cin (1)

Carryout (Cout) = (A xor B)Cin + AB (2)

Shannon Theorem

The Shannon Theorem can be categorized as the function of many variables, f (b0, b1, b2, y, bi, y, bn) can be written as the sum of two terms, say one with a particular variable ai, set to 0, and one with it set to 1.

f (b0, b1, b2, ..., bi,.....y, bn) = bi'f (b0, b1, b2, ..., 0,.....y, bn) + bi f (b0, b1, b2, ..., 1,.....y, bn) (1)

Shannon Based Full Adder

The proposed Shannon full adder circuit as shown in Fig.2 combines the multiplexing operation for the sum operation and the Shannon Theorem for the carry operation; the sum and carry circuits are designed based on Standard full adder equations. An input C and its complement are used as the control signal of the sum circuit. The two-input X-OR gate is developed using the multiplexer method. The output node of the two-input multiplexer circuit is the differential node. According to standard full adder equation, the sum circuits need three inputs. In order to avoid increasing the number of transistors due to the addition of a third input, the following arrangement is made, the CPL X-OR gate multiplying with C's complement input and EX-NOR gate is multiplied with input C, and thereby reducing the number of transistors in the sum circuit. The carry for the half adder is given by

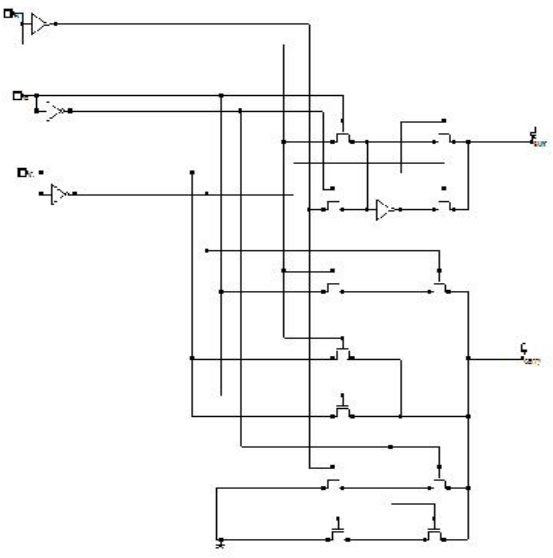


Figure 2: Shannon Based Full Adder

Half Adder

Carry=A.B

Shannon's Theorem

Carry= (A.B) + (B.B')

Full Adder

Sum = A xor B xor C

Sum= ((A xor B).C') + ((A xor B)'.C)

Carry= (A.B) + (B.C) + (C.A)

Carry= (A+B) C + (A.B)

Existing Adder

Carry= (A+B) C + (A.B)+(B'.C')

Proposed Adder 1

Sum= ((A xor B).C') + ((A xor B)'.C)

Carry= (A+B) C + (A.B) + (B'C') + (A'.B')

Proposed Adder 2

Sum= ((A xor B).C') + ((A xor B)'.C)

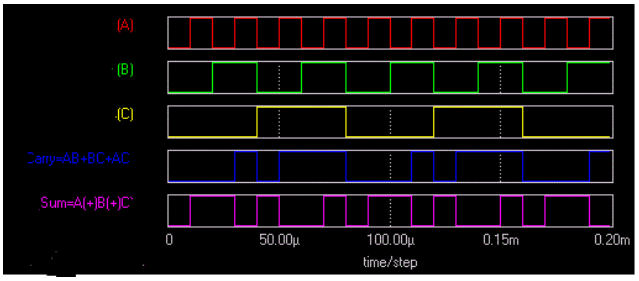
Carry= ((A xor B).C) + ((A xor B)'.A)

C and C' node is called the differential node of the circuit. Two complementary (C and B) inputs are used in the full adder carry circuit for balancing the circuit and to avoid the floating wire concept. In this circuit, all of the pass inputs are connected at VDD line so that the pass gates are always on. The control input terminals are connected to the function inputs. In the proposed adder 2, from Table I instead of giving all the inputs from external input the internal output from the SUM circuitry acts as input to the carry logic. From the truth table it can be found that when A XOR B output is one, the value of Cout is equals to C. When it is zero, the value of Cout is equals to the value of A. In this circuit, there is comparative reduction in the number of transistors and so reduction in Area and power.

Results and Analysis

The existing & proposed architectures are implemented using Full Custom ASIC design methodologies. Both the existing & proposed full

adder architectures were simulated using Tanner tool.



It is interesting to note that power has been reduced. Since it is an architectural innovation, below are the low power advantages:

No Area or Performance penalty.

Minimum Verification effort:

Since it is correct by design.

It is pervasive:

It is independent of adder width.

Conclusion

The proposed Shannon based full adder cell has been simulated and results are compared with existing CMOS based full adder cell in terms of power, transistor count and timing. This proposed adder cell is having improvement in power & transistor count aspects. The proposed low power concept is proven in both ASIC Design Methodologies.

Future Work

In the future work the proposed adder will be used to implement Neural Network. Since adder forms the basic Data path component in the Neural Network. The proposed low power concept will result in the power optimization during both training of the network & normal functioning of the Neural Network. The plan is to develop a servo motor speed control logic based up on Artificial Neural Network.

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Author's details

[1]He received his Bachelor Degree in Electronics and Communication Engg from Haldia Institute of Technology in 2013. Currently he is a student of master degree at Haldia Institute Of Technology in VLSI. Email: getmanish08@gmail.com

[2]Malay K Pandit received his B.E and M. E degrees in Electronics Engineering from Electronics and Telecom Engg Dept, Jadavpur University, India in 1989 and 1991, respectively. He received his PhD from UK's renowned Cambridge University in 1996. He did his post-doc from the Optoelectronics Research Centre, City University of Hong Kong till 2002 where he pioneered the use of polymers for optical waveguide applications. .He then took a corporate career where he worked in a fibre optic company "FONS (I) Ltd" in the domain of optical networking. Now he is a full Professor in the Electronics Engg Dept of the Haldia Institute of Technology where he focuses on embedded systems, including their usage in WDM optical networks. He has 45 international publications in this area.

Dr. Pandit was awarded the National Scholarship of the Government of India in 1983 and the Nehru Scholarship of the Government of India during his Ph.D. studies. Email: mkpandit.seci@gmail.com

[3]Asim K. Jana received his bachelor's and master's degree in electronics Engg from Electronics and Telecom Engg Dept, Jadavpur University, India in 1988 and 1995, respectively. He has 10 years of industrial experience in the domain of embedded systems. Currently he is an associate professor on computer systems. He has 10 international research papers. Email: asimkjana@gmail.com

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