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# Performance Comparison of High-Speed Adders Using 180nm Technology

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**Abstract**

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding binary numbers, it is the nucleus of many other useful operations such as subtraction, Multiplication, division, addresses calculation, etc. In most of these systems the adder is part of the critical path that determines the overall performance of the system. That is why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is a significant goal. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly (doubling every 18 months assuming Moore's Law). At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. The design of an effective cooling system becomes a big major challenge in the VLSI circuit design. This in turn puts constraints on the speed improvement of circuit performance. Therefore, in realizing modern VLSI circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. The objective of our project is to design a high-speed adder, along with lower-power and smaller area as a prime consideration. A Complementary Metal Oxide Semiconductor (CMOS) Transmission Gate (TG) adder and Dual rail-domino full adder are implemented using 180nm technology from Taiwan Semiconductor Manufacturing Company (TSMC).

**Keywords:** Dual Rail domino adder, PDP, Precharge and Evaluation, TG adder

## Introduction

The arithmetic unit is at the heart of any microprocessor, DSP architecture and data processing system. Addition is a basic arithmetic operation and act as the core of other arithmetic operations like multiplication, division, subtraction, address generation etc. The most required feature of modern electronics is low power, energy efficient, building block that enables the implementation of long lasting battery operated systems [1]. There is no a single type of one bit adder which can be used for all type of applications, so, different type of logic styles are used for designing a full adder cell to cover a wide range of performance characteristics to satisfy different applications[2].

For performance analysis of various full adders different parameters are measured like power dissipation, delay, number of transistors used and power delay product of circuit. In a design it is optimised desired that the circuit consume less power, have very less delay, low supply voltage and avoid degradation in output voltage. In the last decades many logic styles have been proposed and each design has its own merits and demerits. It is very important for circuit design to have good drivability under different load conditions and also balanced output to avoid glitches. The time delay depends on size of transistors, number of transistors used, logic depth, parasitic capacitance and capacitance due to intercell and intracell routing and also on number of inversion levels. Power dissipation

depends on switching activity, the number and size of transistors, node capacitance, wiring complexity etc[3].

$P_{avg} = P_{static} + P_{dynamic} + P_{short\text{-}circuit}$

The energy consumed by gate per switching element is known as PDP. The power delay product is a measure of efficiency in an adder circuit. There is a tradeoff between power dissipation and speed and is very important when low power operations are needed. It is given by

PDP =Power * DELAY

Reducing the number of transistors may lead to reduced power but sometime does not improve. The die area depends on number and size of transistors and routing complexity. All these characteristics of full adder vary from one logic to another logic[2]. In this paper two full adders namely transmission gate full adder and dual rail domino full adder are compared at transistor level using 180nm CMOS technology.

**Truth table and equation**

A full adder performs the addition of two bits A and B with the Carry (Cin) bit generated in the previous stage [4]. The integer equivalent of this relation is shown by:

$A+B+Cin = 2*Cout+Sum$ (1)

The conventional logic equation for Sum and Carry are;

$Cout = (A . B) + (A+B) .Cin$ (2)

$Sum = (A .B .Cin) +(A+B+Cin) . \overline{Cout}$ (3)

The truth table for full adder is as follows:

Table 1: Truth table

| A | B | Cin | Sum | Cout |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Design technologies**

***A) Transmission gate adder***

A transmission gate consists of an nMOS transistor and a pMOS transistor in parallel with gates controlled by complementary signals. When the transmission gate is ON, at least one of the two transistors is ON for any output voltage and hence, the transmission gate passes both 0s and 1s well. The transmission gate is a fundamental and ubiquitous component in MOS logic [6]. It finds use as a multiplexing element, a logic structure, a latch element, and an analog switch. The transmission gate acts as a voltage-controlled switch connecting the input and the output. A single nMOS or pMOS pass transistor suffers from a threshold drop. If used alone, additional circuitry may be needed to pull the output to the rail [5]. Transmission gates solve this problem but require two transistors in parallel. A rather different full adder design uses transmission gates to form multiplexers and XORs.

Figure 3 shows the transistor-level schematic using 26 transistors and providing buffered outputs of the proper polarity with equal delay. The design can be understood by parsing the transmission gate structures into multiplexers and an "invertible inverter" XOR structure as drawn in Figure. 1 [7]. Transmission gate logic circuit is a special kind of pass-transistor logic circuit. The main disadvantage of transmission gate logic is that it requires twice the number of transistors than pass-transistor logic or more to implement the same circuit. The gate level implementation of transmission gate full adder using NAND gates and multiplexer is shown in figure 1. In figure 2 the NAND gates and multiplexers are replaced with transmission gates.

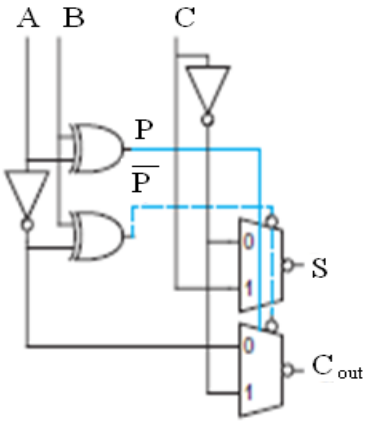


Figure 1: Gate level implementation

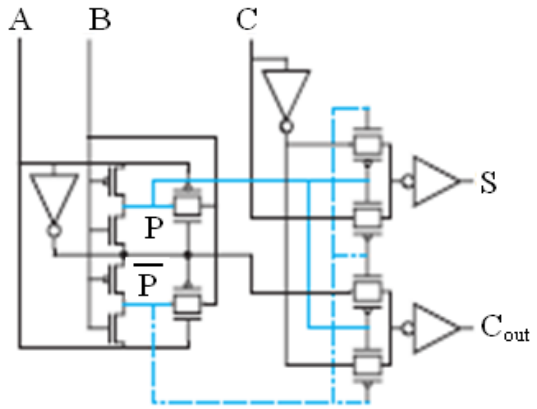


Figure 2: Gate replaced with transmission gate

Figure 3 shows the implementation of transmission gate full adder with transmission gates and CMOS transistors. Since transmission gate requires twice the number of transistors to implement same circuit this adder cell uses 26 transistors. TG (also called CMOS CPL logic in many cases) has the ability of a high-quality switch with low resistance and capacitance. It is one of the members of the ratioless logic family as the DC characteristics are independent of the input levels. Sizing is also not necessary in general, as the resistance and capacitance decrease and increase respectively as the gate W=L ratio is increased [8]. TG is commonly used to implement of XORs and MUXs with the minimum number of transistors.

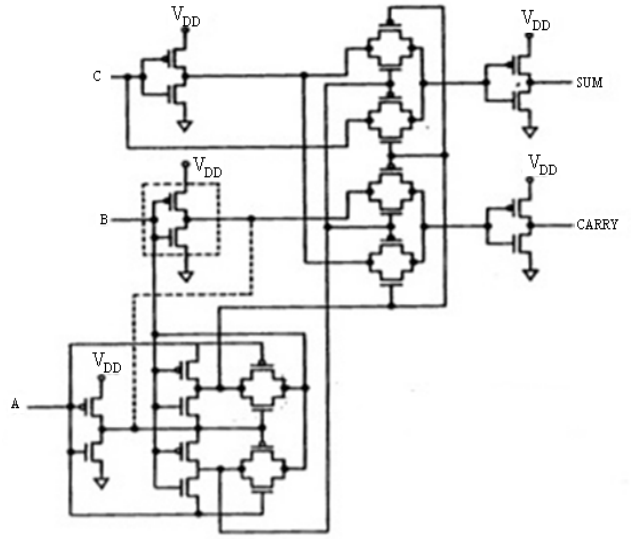


Figure 3: Transistor level implementation

Transmission gate full adder has good delay, power dissipation and PDP than CCMOS and CPL. It gives better speed than static CMOS, CPL and requires less number of transistors. It has high number of internal nodes which leads to an increase in parasitic capacitance. In large arithmetic circuits it gives poor performance. Additional buffers are required at each output due to their week driving capability which increases power consumption and area.

**B) *Dual - rail domino logic***

Ratioed circuits reduce the input capacitance by replacing the pMOS transistors connected to the inputs with a single resistive pullup. The drawbacks of ratioed circuits include slow rising transitions, contention on the falling transitions, static power dissipation, and a nonzero VOL. Dynamic circuits circumvent these drawbacks by using a clocked pullup transistor rather than a pMOS that is always ON. Figure 4 shows a simple dynamic inverter circuit.

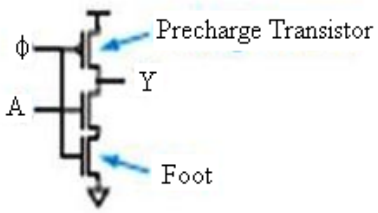


Figure 4: Dynamic inverter

Dynamic circuit operation is divided into two modes, as shown in Figure 5. During precharge, the clock is 0, so the clocked pMOS is ON and initializes the output Y high. During evaluation, the clock is 1 and

the clocked pMOS turns OFF. The output may remain high or may be discharged low through the pulldown network.

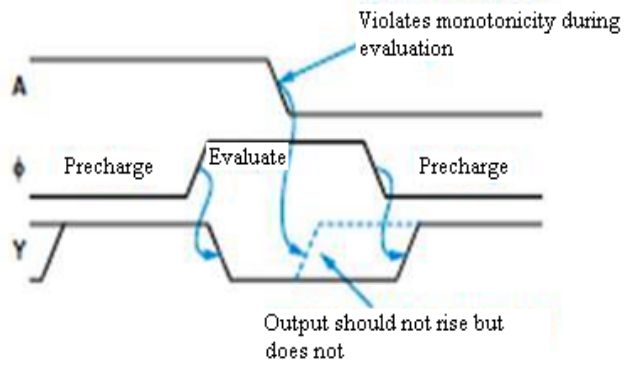


Figure 5: Waveform of dynamic inverter

Dynamic circuits are the fastest commonly used circuit family because they have lower input capacitance and no contention during switching. They also have zero static power dissipation. However, they require careful clocking, consume significant dynamic power, and are sensitive to noise during evaluation. If the input A is 1 during precharge, contention will take place because both the pMOS and nMOS transistors will be ON. When the input cannot be guaranteed to be 0 during precharge, an extra clocked evaluation transistor can be added to the bottom of the nMOS stack to avoid contention.

A fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. That is, the input can start LOW and remain LOW, start LOW and rise HIGH, start HIGH and remain HIGH, but not start HIGH and fall LOW. Figure 5 shows waveforms for a footed dynamic inverter in which the input violates monotonicity. During precharge, the output is pulled HIGH. When the clock rises, the input is HIGH so the output is discharged LOW through the pulldown network, as you would want to have happen in an inverter. The input later falls LOW, turning off the pulldown network. However, the precharge transistor is also OFF so the output floats, staying LOW rather than rising as it would in a normal inverter. The output will remain low until the next precharge step. In summary, the inputs must be monotonically rising for the dynamic gate to compute the correct function. Unfortunately, the output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation [5].

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates. This converts the monotonically falling output into a monotonically rising signal suitable for the next gate. The dynamic-static pair together is called a domino gate, because precharge resembles setting up a chain of dominos and evaluation causes the gates to fire like dominos tipping over, each triggering the next. A single clock can be used to precharge and evaluate all the logic gates within the chain. The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising. Domino gates are inherently non-inverting, while some functions like XOR gates necessarily require inversion. Three methods of addressing this problem include pushing inversions into static logic, delaying clocks, and using dual-rail domino logic [5].

In many circuits including arithmetic logic units (ALUs), the necessary XOR gate at the end of the path can be built with a conventional static CMOS XOR gate driven by the last domino circuit. However, the XOR output no longer is monotonically rising and thus cannot directly drive more domino logic. Dual-rail domino gates accept both true and complementary inputs and compute both true and complementary outputs, as shown in Figure 6 which shows the Dual – rail domino implementation of XOR gate.

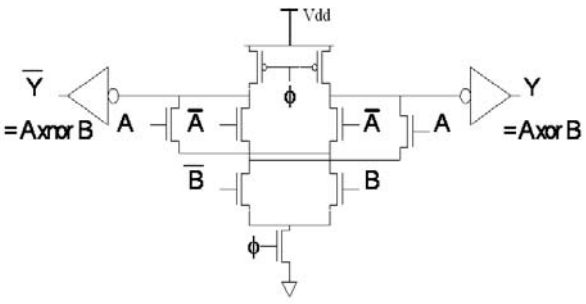


Figure 6: Dual– rail domino XOR

The gates are shown with clocked evaluation transistors, but can also be unfooted. Dual-rail domino is a complete logic family in that it can compute all inverting and non-inverting logic functions. However, it requires more area, wiring, and power. Dual-rail structures also lose the efficiency of wide dynamic NOR gates because they require

complementary tall dynamic NAND stacks. Dual-rail domino signals not only the result of a computation but also indicates when the computation is done. Before computation completes, both rails are precharged. When the computation completes, one rail will be asserted. A NAND gate can be used for completion detection. This is particularly useful for asynchronous circuits [9].Dynamic logic uses a sequence of pre-charging and conditional evaluation phases to realize complex logic functions in a single NMOS pull-down or PMOS pull-up network, hence this requires less transistors and also has no static power consumption. The reduced overall capacitance results in significantly improvement in the speed. The disadvantage of dynamic logic is the high dynamic power dissipation due to clock switching. Furthermore, the dynamic logic has clock skew and charge-sharing problems. The dynamic logic style would be implemented in applications where performance is the primary concern. The main types of dynamic logic are Domino, NP-CMOS, and True Single-Phase Clocked Logic (TSPCL). The C2MOS latched NP-CMOS (also called NORA-CMOS) can be used in the effective implementation of pipelined circuits. The dual rail domino full adder is shown in figure 7, which has a high noise immunity, reduced capacitance at the dynamic output, high speed and occupies less area.

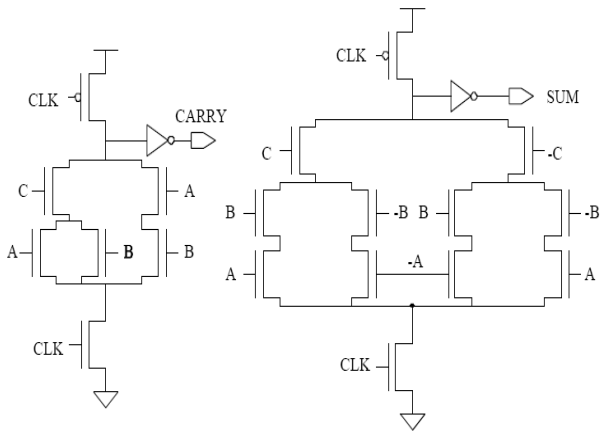


Figure 7: Dual– rail domino full adder

**Main results**

Table 2: Simulation results

| Adder | No. of transistors | Total power consumption | Delay (ns) | PDAP (e-20) |
|---|---|---|---|---|
| 26 TG | 26 | 173.7870pW | 0.0911 | 41.163 |
| Dual rail domino | 23 | 46.363pW | 0.0692 | 7.3834 |

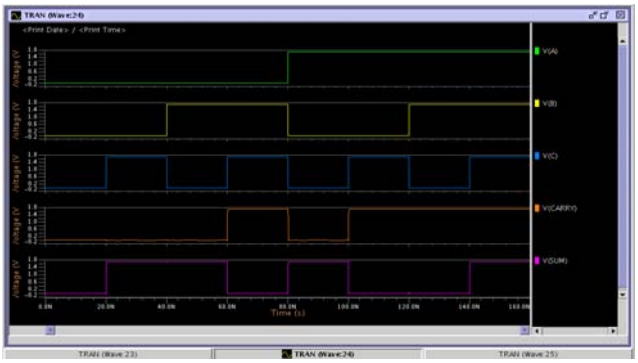

Figure 8: Resultant wave for 26 TG

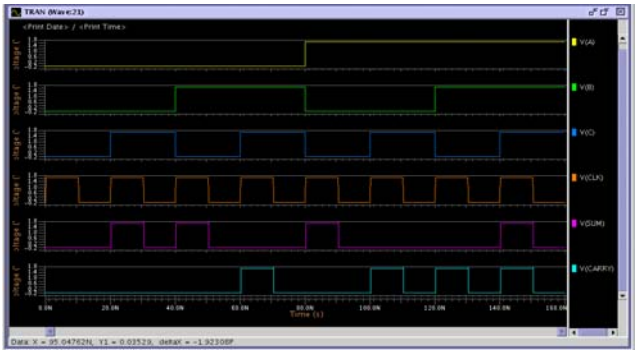

Figure 9: Resultant wave for Dual rail domino

**Conclusion**

The project describes, the speed of a circuit depends on the size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. After simulating the adders we find that the power consumption of the circuit increase with increase in the number of transistors, also the delay for dual rail domino is less. Finally the calculated PADP, and found that the PDAP of dual rail domino is less.

Therefore a tradeoff between power consumption and delay is necessary to design a circuit.

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