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Optimized Low Power 8-bit Array Multiplier with CSA and CLA

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Abstract- This paper presents an optimized design of an 8-bit array multiplier optimized for superior performance and reduced power usage. While conventional array multipliers are straightforward to design, they often suffer from high propagation delays and excessive power demands. The proposed design integrates Carry Save Adders (CSA) for parallel partial product summation and Carry Look-Ahead Adders (CLA) for efficient final addition. Simulations confirm the design's improved speed, lower power consumption, and better area efficiency, making it an ideal choice for mobile and embedded applications. The architecture was implemented using Verilog HDL and validated with Xilinx Vivado tools on the Artix7 platform, demonstrating its practicality The design is implemented in Verilog HDL and simulated using Xilinx Vivado, showcasing the practical viability of the architecture.

Keywords- Array Multiplier, Low Power Design, High Performance, Carry-Save Adders, Carry Look-Ahead Adders, Verilog HDL, Xilinx Vivado.

I. INTRODUCTION

Multiplication is a core arithmetic operation essential in numerous digital systems, including processors and other application-specific systems. Efficient multiplier designs are crucial for advanced hardware to achieve high performance while minimizing power consumption. This multiplier is significant for applications as it offers high-speed computation with low energy consumption. While many array multipliers are simple to implement and easy to design, they often encounter several challenges, such as high power consumption, long propagation delays, computation errors, and other pitfalls faced in normal array multipliers. These issues become more pronounced as the bit-width of the operand increases.

This study introduces an 8-bit array multiplier enhanced design for performance and low power consumption, incorporating Carry Save Adders (CSAs) and Carry Look-Ahead Adders (CLAs). This design enhances power efficiency and speed, reducing latency and power consumption, making it suitable for resource-constrained systems. The focus is designing an 8-bit array multiplier that minimizes power consumption without compromising performance, striving for an optimal balance between speed and energy efficiency. We assessed the proposed multiplier through simulation, benchmarking its performance against various designs based on power consumption, delay, and area. The results demonstrate that the proposed multiplier achieves substantial power savings while preserving high performance, making it well-suited for low-power applications. This indicates that array multipliers can be optimized for energy efficiency without sacrificing performance, offering a practical solution for low-power embedded systems, mobile devices, and other power-critical applications.

II. LITERATURE REVIEW

Significant efforts are underway worldwide to design multipliers optimized for low-power VLSI applications. This section provides a summary of recent progress in multiplier designs aimed at enhancing energy efficiency

In [1]Design and Analysis of 8-bit Multiplier for Low Power VLSI Applications, the study focuses on optimizing power consumption and performance in an 8-bit multiplier by using traditional full adder architectures and ripple carry adders, While the design achieves reductions in power and delay, it encounters challenges in scalability and performance when dealing with higher bit-width multiplications, resulting in increased latency and higher power consumption.

In [2] a bottom-up temporal tiling approach is proposed to enhance array multiplier performance by visualizing and compacting delays in two-dimensional circuits. The resulting leapfrog array multiplier improves speed and power, it results in increased metal usage, which could increase costs or complexity in fabrication.

The proposed design leverages advanced adder techniques, such as Carry Save Adders (CSAs) and Carry Look-Ahead Adders (CLAs) to optimize the 8-bit array multiplier. This approach significantly improves speed and reduces power consumption, making it ideal for high-performance and low-power applications. Unlike traditional designs that face scalability issues and increased latency with larger bit-width multiplications, this design remains efficient even with larger operands. Furthermore, it avoids the challenge of increased metal usage seen in other architectures, offering a more fabrication-friendly solution for resource-constrained systems like mobile and embedded devices.

Multipliers and Their Implementations

Multipliers are crucial components in digital systems, with various types designed to optimize speed, power, and area based on the specific application. Digital logic design encompasses utilizing the set of logic gates and memory elements to create complex systems that perform operations and store data. Effective design requires balancing trade-offs between speed, power, and area while ensuring functionality and efficiency.

Traditional Array Multipliers:

Traditional array multipliers employ a simple approach where partial products are generated and summed using a grid of adders, typically consisting of full adders and half adders. In this method, each bit of one operand is multiplied by each bit of the other, resulting in partial products that are aligned and added together to produce the final product. While this approach is straightforward to design and implement, It requires a large number of logic gates, leading to substantial power consumption and propagation delays, particularly as the bit-width increases The main drawbacks of this multiplier include:

- High power consumption
- Propagation delay

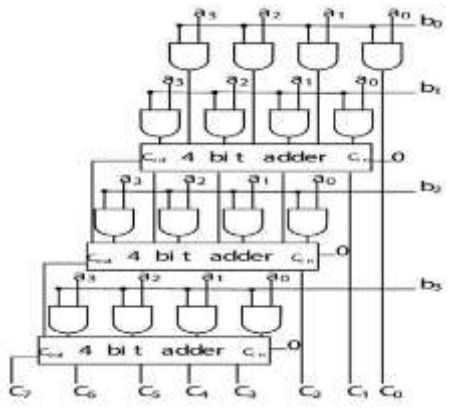

Fig 1 Traditional Array Multiplier

Conventional 8-bit array Multiplier

This conventional multiplier is designed to achieve faster multiplication using full adders and combinational logic circuits. It generates partial products through multiplication, with the bits processed sequentially, leading to quicker output. The inputs are added together, producing both sum and carry, This approach improves output speed by

reducing the preprocessing time. The main drawbacks of this multiplier include:

- High power consumption
- Long Propagation delay
- Potential computation errors

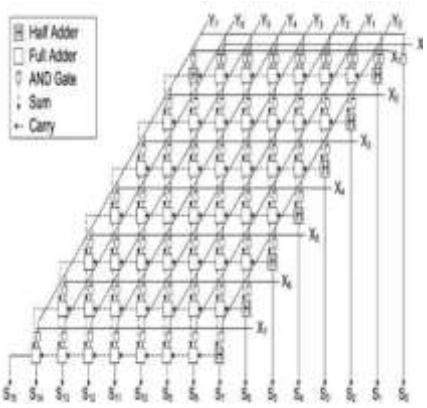

Fig 2 Conventional array multiplier

III. PROPOSED DESIGN

This paper presents an optimized 8-bit array multiplier for low power and high performance. The proposed design improves computation speed while reducing power consumption. It leverages Carry- Save Adders(CSAs) and Carry Look-Ahead adders (CLAs) to enhance both speed and efficiency.

The implementation of the proposed design is as follows:

Partial Product Generation:

The first step follows the basic principle of array multiplier, partial products are obtained by multiplying the individual bits of two operands. In an 8-bit multiplier, each bit of one operand is multiplied by each bit of the other, generating 64 partial products. The mathematical operation can be represented as:

$Pi=Ai \times Bj$ for $i, j \in \{0,1,2,...,7\}$

Ai and Bj are the bits of operands A and B, and Pi represents the partial product generated at each stage.

Partial Product Summation Using Carry -Save Adders (CSA):

In this step, the partial products generated in the previous stage are summed using Carry-Save Adders (CSAs). Unlike ripple-carry adders (RCAs), CSAs allow multiple partial products to be added simultaneously without immediately propagating carry bits instead, the carry bits are saved and are propagated only after all partial sums are calculated. The mathematical operation performed by the CSA is as follows:

Si = Pi + Ci (sum of partial products)

C carry = carry bits saved for later propagation

Final Summation Using Carry Look- Ahead Adders (CLA):

Once the CSA stage reduces the number of partial products, the final summation is performed using carry look-ahead adders (CLAs). CLAs precompute carry bits in parallel, determining whether a carry will propagate through each stage, This significantly reduces the delay in the final summation stage. The final addition operation can be represented as:

Final Sum = Sum of (Si +C carry)

Where Si are the Intermediate sums and Ccarry are the carry bits propagated by the CLA.

Low- Power Techniques:

To minimize power consumption, several low-power techniques are integrated into the design.

- **Clock gating:** Deactivates unused parts of the multiplier when not in use, reducing dynamic power consumption
- **Operand Isolation:** Disables parts of the multiplier not involved in the current calculation, reducing switch activity and dynamic power.
- **Dynamic Voltage Scaling (DVS):** Adjusts the supply voltage to reduce power consumption during periods of low computational demand.
- **Transistor-level Optimization:** Optimizes transistor sizing and utilizes low-power design techniques to minimize leakage current and static power

Block Diagram

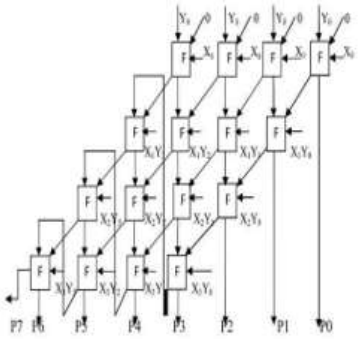

Fig 3 Array multiplier using CSA and CLA

Work Flow

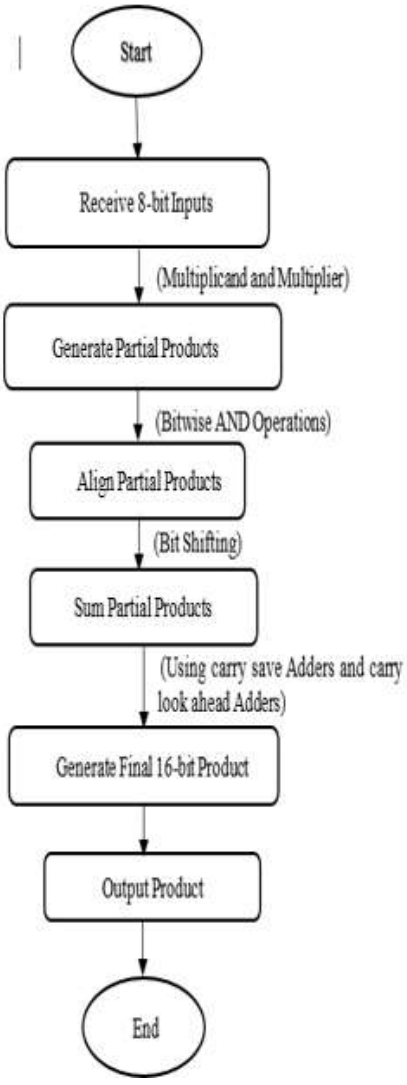

Fig 4 Workflow of the proposed design

Schematic diagram

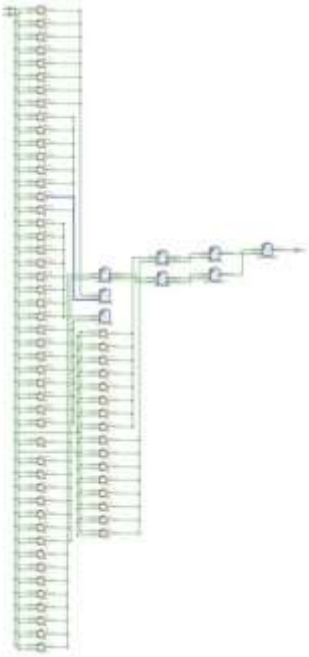

Fig 5 Schematic diagram of the proposed design

Simulation Results

Fig 5 Simulation Results of Proposed Design

Power Consumption Results of proposed design

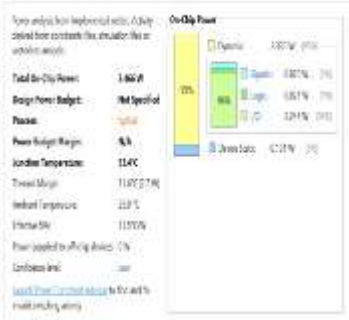

Fig 6. Power Consumption Results of Proposed Design

Comparison of Multipliers

Parameter	Speed(ns)	Power consumption(W)	Area(um)
Traditional Array multiplier	1	36	1
Computational Array multiplier	1.5	9.201	0.9
Array multiplier using (CSA and CLA)	1.2	2.466	0.8

Fig 7. Comparison of multipliers

Graphical Analysis of the Comparison

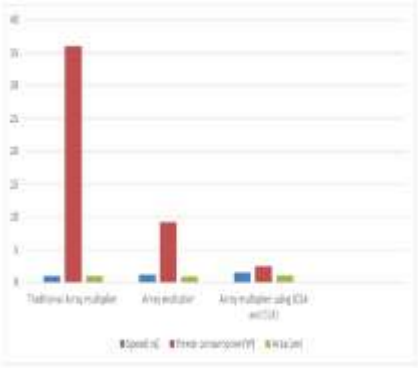

Fig 8 Graphical Analysis of the Comparison

IV. RESULTS AND DISCUSSION

The optimized 8-bit array multiplier, designed using Verilog HDL and simulated in Xilinx Vivado, was tested on the Artix7 evaluation board. This design enhances three critical factors: delay, power consumption, and area.

Delay

The use of carry-save adders (CSAs) and Carry Look-Ahead Adders (CLAs) Reduces delay by deferring carry propagation, which leads to faster multiplication

Power Consumption

Power is minimized through techniques like clock gating, operand isolation, and dynamic voltage scaling, achieving significant reductions in dynamic power.

Area

While CSAs and CLAs add hardware complexity, they improve speed and power efficiency, making the increase in area worthwhile.

V. CONCLUSION

The proposed optimized 8-bit array multiplier using CSAs and CLAs provides a high-performance and low-power solution suitable for mobile applications and embedded systems. The design significantly reduces delay and power consumption while enhancing efficiency.

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