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Efficient Design And Implementation Of Low-Power Full Adder Circuits Using Cmos Technology

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Abstract- This study compares the design of one-bit full adder circuits with 14-transistor and 22-transistor versions using CMOS technology. Its main goals are speed improvement and power consumption reduction. Discussions are held regarding design techniques, testing configurations, and output outcomes. Circuits that use XOR and XNOR are also assessed. The suggested designs provide improved speed and power efficiency, according to the results. Implementation is done with Cadence Virtuoso.

Keywords- Full adder, XOR, XNOR, MOSFET, CMOS AND CADENCE VIRTUOSO.

I. INTRODUCTION

Full adders represent essential building blocks of digital arithmetic. As electronic devices became more demanding in terms of power consumption and speed, designing adders with lower power consumption and higher speed became necessary. Such designs are ideally suited for CMOS technology. This paper discusses design and analysis of one-bit full adder CMOS circuits and comparison of two circuits introduced here, namely 22T and 14T. The goal is to improve performance with minimal power and area overhead. Cadence Virtuoso is used to test and verify the designs.

II. PROBLEM STATEMENT

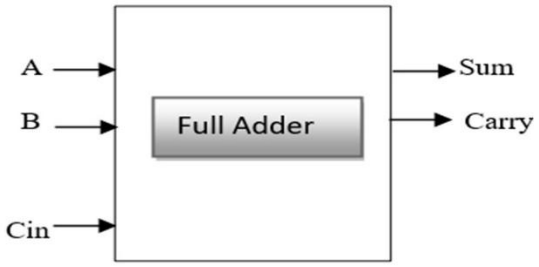
In contemporary digital electronics, full adders are basic building blocks employed in processor arithmetic operations, ALUs, and other digital systems. As technology shrinks and handheld devices become more common, minimizing power consumption and maximizing speed has become a major challenge for circuit designers. Conventional full adder designs, though functionally good, tend to employ many transistors, which contributes to increased chip area, power consumption, and delay—making them less desirable for low-power and high-speed applications. CMOS technology, with its low static power dissipation and high noise immunity, promises an effective solution for the optimal design of digital circuits. But getting the proper balance of power, speed, and area in CMOS full adder circuits is still a challenging job.

This study seeks to resolve this problem by creating and simulating two distinct CMOS-based one-bit full adder circuits: one with 22 transistors and a more optimized circuit with 14 transistors. The objective is to compare and evaluate their performance in power consumption, delay, and silicon area using Cadence Virtuoso for simulation and verification. The research aims to identify if minimizing the number of transistors may result in an efficient full adder design that does not reduce functionality and reliability.

III. FULL ADDER

A full adder calculates the sum of three binary bits that include the carry-in from the previous stage, the addend, and the augend. Full adders are relatively stronger than half adders in computation since they can use the complexity of the carry in input into the addition of multiple bits. A half adder sums two bits only, but a full adder has two outputs: the sum of the three bits and the carry-out (Cout), passed on to the next stage. As full adders can have more than one

input, they are crucial in producing accurate and efficient binary addition in circuits.



$$Sum = A \oplus B \oplus Cin \quad (1)$$

$$Cout = AB + (A \oplus B).\ Cin \quad (2)$$

Full Adder

A	B	C	C Out	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Table -1: Truth Table

IV. CMOS 14T Full Adder

The XNOR and XOR modules are used to obtain the adder's sum output. PMOS and NMOS transistors make up the inverter, which inverts the input logic. By combining robust transmission gates with CMOS inverters for a 1.8V supply, the circuit's average power was reduced using 90-nm technology.

V. DESIGN AND ANALYSIS OF FULL ADDER:

The task is to generate an effective full adder design needed to achieve the performance requirements of an application. The full adder performs the addition of binary digits with a carry input and generates a sum and a carry output for the next stage. In this paper, the adder has been designed with a minimum transistor count, 14-transistor (14T), thus combining the advantages of low transistor count and better efficiency. The design is synthesized in Cadence Virtuoso in 90nm technology to match contemporary semiconductor processes. The performance is tested by simulating parameters like power dissipation, propagation delay, and overall power consumption. A comparative analysis is done to assess the performance suitability of the design for low-power and high-speed application.

14t Full Adder

A 14T full adder is a digital circuit designed using 14 transistors to perform the arithmetic operation of binary addition. It adds three input bits: two significant bits (A and B) and a carry-in (Cin), producing a sum (S) and a carry-out (Cout). The goal of a 14T design is to reduce the number of transistors while maintaining functionality and performance, making it more power-efficient and suitable for low-power VLSI applications. Compared to conventional full adders, the 14T design reduces area, power consumption, and delay, making it an attractive choice for portable and embedded systems. However, trade-offs such as reduced noise margins or degraded signal levels may occur depending on the transistor-level implementation.

14-Transistor schematic design

The 14-transistor (14T) schematic design is a compact and efficient implementation of a full adder circuit, using only 14 MOS transistors. This design focuses on minimizing the number of components to save chip area, reduce power consumption, and improve overall speed. The 14T full adder typically combines pass transistor logic (PTL) and complementary MOS (CMOS) techniques to achieve this optimization. It generates the intermediate signals required for sum and carry functions with fewer switching elements, which leads to lower dynamic power usage. Despite the reduction in transistor count, the 14T design maintains acceptable performance for many applications, especially in low-power VLSI systems. However, it may suffer from issues such as voltage degradation and limited driving capability, which require careful design considerations to ensure reliable operation in practical circuits.

Wave forms

Waveforms are graphical representations of how signals change over time in an electrical or electronic circuit. In digital systems, waveforms typically show voltage levels that represent binary values (0 and 1), making them essential for analyzing the behavior of logic circuits such as full adders. These waveforms illustrate the timing relationship between input signals (like A, B, and Cin) and the resulting output signals (Sum and Cout). By examining waveforms, engineers can verify the correctness of a circuit, identify timing issues, and understand how signals propagate through various logic gates. In a 14-transistor full adder, waveforms help visualize the response of the circuit to different input combinations, ensuring that the sum and carry outputs are generated accurately and without delay faults. They are a crucial part of simulation and debugging in digital design.

Conclusion

Low power one-bit full adder circuit implementation with 22 transistors and optimal use of 14 transistors were explored in this work. Power efficiency, speed, and area efficiencies were compared based on two architectures. The evidence confirms that minimal transistors will lead to remarkable power improvement with the requisite operation speed still intact. The CMOS-based designs under consideration are more efficient for high-speed and low-power applications. Cadence Virtuoso simulations confirm the correctness and performance of the circuits and demonstrate the merits of using reduced-transistor full adder circuits in contemporary digital systems. The research adds to the continuing process of improving digital circuits for high-performance, energy-efficient applications.

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