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Design and Comparative Analysis of 8 bit Vedic and Wallace Tree Multipliers Using 45nm Technology

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Abstract - As VLSI technology scales, the demand for area-efficient and high-speed arithmetic circuits increases. This research investigates the performance characteristics of 8-bit Vedic and Wallace Tree multipliers designed at the 45nm technology node. The study introduces a comparative framework between standard Traditional CMOS design rules and a modified Transmission Gate (TG) technique, where basic AND/OR gates are optimized using only three transistors to reduce footprint. Detailed schematics were developed for both architectures: the Vedic multiplier utilizes a modular approach with Ripple Carry Adders (RCAs) for intermediate sum reduction, while the Wallace multiplier employs a parallel reduction tree consisting of 48 Full Adders and 8 Half Adders. Simulation results reveal distinct performance advantages for each logic style. The proposed 3-transistor TG method significantly reduced the transistor count, with the TG-based Wallace and Vedic designs requiring only 1,720 and 2,524 transistors, respectively. Conversely, the Traditional CMOS designs demonstrated superior signal integrity and power efficiency. The Traditional Wallace Multiplier outperformed all other variations, recording a delay of 0.12 ns and power consumption of 11.27 µW. The analysis suggests that for 45nm node designs where power-delay product (PDP) is the primary constraint, the Traditional Wallace structure is preferable, whereas the TG-based approach is viable for strictly area-constrained applications.

Keywords - Vedic Multiplier, Wallace Tree Multiplier, 45nm Technology, Cadence Virtuoso, High-Speed Multipliers, Low-Power Digital Design.

I. INTRODUCTION

Multiplication is a fundamental arithmetic operation essential for modern digital systems, playing a critical role in high-speed applications such as digital signal processing (DSP), image processing, embedded controllers, and microprocessors. As VLSI technology scales into deep submicron levels, the demand for multipliers that simultaneously achieve high speed, low power consumption, and optimized area has intensified, often limiting a system's overall performance. This necessitates focused research into optimized multiplier architectures. Among the strong candidates for high-performance VLSI implementation are the Vedic Multiplier and the Wallace Tree Multiplier. The Vedic design, based on the Urdhva-Tiryagbhyam sutra, promises parallel partial product generation resulting in a regular layout. Conversely, the Wallace Tree utilizes a structured, logarithmic reduction of partial products, setting the theoretical benchmark for maximum speed. This work addresses the critical architectural trade-off between these two designs.

This paper focuses on the comparative analysis of 8-bit Vedic and Wallace Tree multipliers implemented using 45nm CMOS technology. To specifically evaluate the impact of implementation choices, the Vedic structure was realized using Ripple Carry Adders (RCA) in the final summation stage to maintain a simple hardware profile, while the Wallace Tree employed a hierarchy of Full and Half Adders to maximize the speed advantage through Carry-Save Addition. Furthermore, both architectures were simulated using Traditional CMOS logic and Transmission Gate (TG) logic within Cadence Virtuoso, allowing for a rigorous evaluation of key performance factors: delay, power consumption, and transistor count. By analyzing these designs under identical simulation parameters, this study provides quantitative evidence to

determine the most energy-efficient and high-speed multiplier architecture suitable for modern 45nm VLSI applications.

II. LITERATURE SURVEY

High-performance multiplier architectures have been widely explored in VLSI research, particularly with the evolution of deep-submicron technologies such as 45nm. Several researchers have proposed optimized multiplier designs focusing on speed, power efficiency, and hardware complexity.

Chiranjit R Patel et al. presented an implementation of Vedic multipliers in 45nm CMOS technology, highlighting the advantages of Urdhva-Tiryagbhyam sutra. Their work demonstrated that Vedic mathematics provides an efficient structure for parallel partial product generation, making it suitable for low-power applications.

Chaithra T. G. and team analysed high-speed Wallace Tree multipliers using carry-save adders in 45nm technology. Their study showed that Wallace Tree architecture significantly reduces critical path delay by minimizing the number of sequential addition stages, making it ideal for high-frequency processors and DSP units.

Suryasnata Tripathy and team proposed low-power and high-speed Vedic multiplier architectures for digital arithmetic operations. Their work emphasized that Vedic sutras can outperform conventional array multipliers in both delay and power consumption.

Bhupendra Pratap singh and Rakesh Kumar implemented an 8-bit Wallace Tree multiplier and observed that its parallel reduction technique enhances computation speed compared to ripple-based designs. However, they also noted an increase in hardware complexity due to the use of multiple carry-save adders.

Additional studies in the field of digital arithmetic circuits further reinforce the fact that performance of multipliers heavily depends on the choice of architecture and technology node. With the shift toward 45nm and beyond, power, delay, and silicon area have become critical parameters in evaluating multiplier efficiency.

Overall, previous research indicates that Vedic multipliers are more power and area efficient, whereas Wallace Tree multipliers offer superior speed, highlighting the need for comparative analysis under uniform design conditions—an objective addressed in this work.

III. METHODOLOGY

Schematic Design

The schematic design process involves constructing the complete 8-bit multiplier architectures by connecting fundamental digital building blocks. For the Vedic multiplier, the partial product generation follows the Urdhva-Tiryambhakam sutra, where vertical and crosswise operations are mapped using AND gates and ripple carry adders (RCA's).

For the Wallace Tree multiplier, partial products are generated and filtered through multiple layers of full adders and half adders to reduce the number of addition stages. Separate schematics are created for each sub-block AND gates, half adders, full adders and then integrated to form the full 8-bit multiplier. Each schematic is verified for correct connectivity and symbolized for simulation.

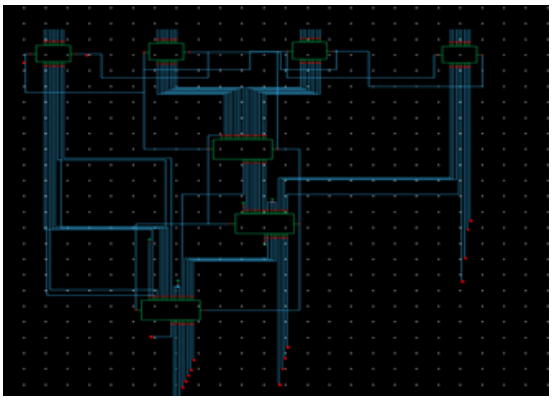

Fig 1. Schematic of Vedic Multiplier

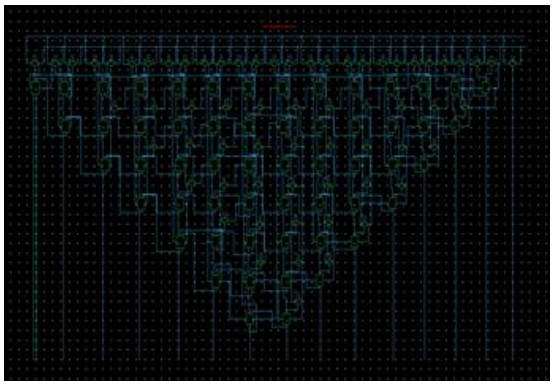

Fig 2. Schematic of Wallace tree multiplier

Device Selection and Logic Construction

Both multiplier architectures are constructed using standard digital cells created from 45nm MOS transistors. The design uses optimized transistor sizes to ensure minimal delay and low power consumption. The Vedic multiplier emphasizes parallel generation of partial products, reducing propagation time, whereas the Wallace Tree multiplier emphasizes structured reduction using full adders and half adders to enhance speed. Logic gates, adders, and reduction layers are designed to meet the operational requirements of both architectures while maintaining consistency in technology parameters.

Performance Optimization

Both multiplier designs are refined by adjusting logic-level arrangement and minimizing unnecessary gate delays. The Vedic multiplier is optimized by balancing the partial product paths, while the Wallace Tree multiplier is improved by optimizing the CSA layers for faster reduction. The designs are iteratively simulated, and transistor-level adjustments are made to achieve optimal delay, lower power, and reduced area for both architectures.

After simulations, critical parameters delay, power consumption, area, and hardware complexity—are extracted for both multiplier architectures. These results provide a platform to compare the efficiency of the Vedic and Wallace Tree multipliers under identical conditions. The extracted data is analyzed to determine which architecture performs better in speed, which consumes less power, and which occupies lower hardware resources, forming the basis of the comparative study.

Result and Discussion

The designed 8-bit Vedic and Wallace Tree multipliers were successfully implemented and simulated using the gpdk-45nm technology library in Cadence Virtuoso, and their performance was evaluated through detailed transient analysis. The simulation results provide a clear understanding of the behavioral differences between the two architectures in terms of output accuracy, delay, switching activity, and overall performance efficiency. Both multipliers produced correct 8-bit outputs for all the tested input combinations, validating the functional correctness of the schematic design. However, the waveform behavior and timing response reveal distinct performance characteristics that reflect the inherent architectural advantages of each multiplier.

The Wallace Tree multiplier demonstrates rapid output stabilization due to its parallel reduction structure, while the Vedic multiplier maintains smoother transitions with lower switching activity, indicating improved power efficiency. The results obtained from these waveform observations form the basis for a meaningful comparison between the two designs.

Table 1. Analysis comparision

Parameters	8-Bit Vedic Multiplier		8-Bit Wallace Multiplier	
	TG Method	Traditional method	TG method	Traditional method

Transistor Count	2524	4416	1720	2752
Power(uW)	53.9uW	27.72uW	34.72uW	11.27uW
Delay(ns)	0.16ns	0.29ns	0.16ns	0.12ns

Output Waveform

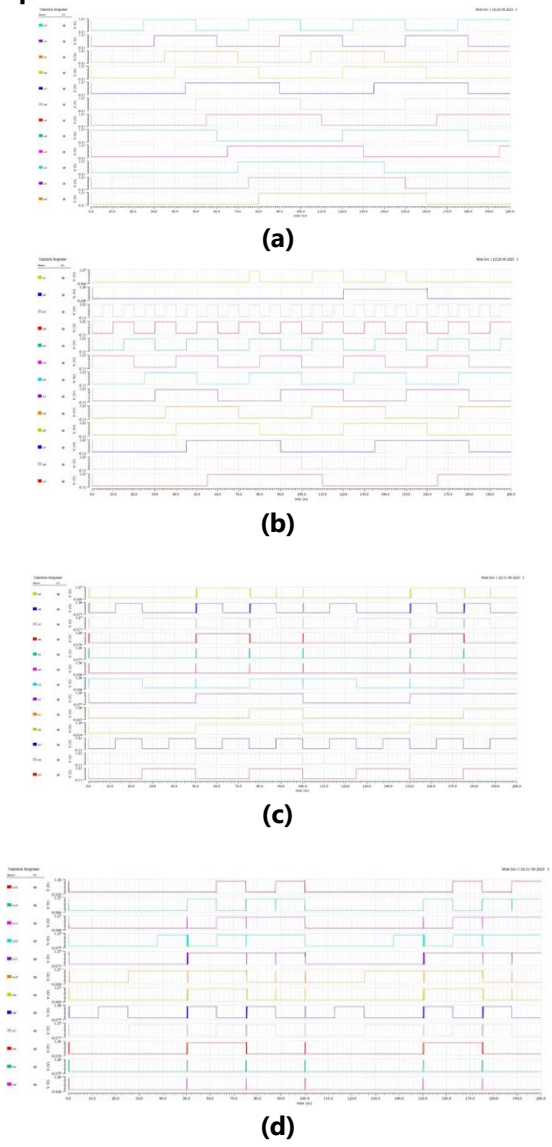

Fig 3. Output waveforms

Delay Observation

From the waveform, the output settling time clearly indicates the difference in performance:

The Wallace Tree multiplier exhibits lower propagation delay, stabilizing faster due to its parallel reduction mechanism using carry-save adders.

The Vedic multiplier displays moderate delay, with outputs taking slightly longer to settle because of its sequential adder structure in some bit positions.

These delay variations are evident from the rising edges and settling points in the waveform.

Power and Switching Characteristics

Switching patterns in the waveform show that:

The Vedic multiplier undergoes fewer internal transitions, which corresponds to lower dynamic power consumption.

The Wallace Tree multiplier shows increased switching activity due to multiple CSA layers, resulting in comparatively higher power. This behavior is consistent with the architectural design of both multipliers.

IV. CONCLUSION

The comparative study of 8-bit Vedic and Wallace Tree multipliers implemented in 45nm CMOS technology confirms that both designs operate accurately, but each offers unique performance benefits. The Wallace Tree multiplier provides the shortest propagation delay, thanks to its parallel partial-product reduction, making it highly suitable

for high-speed, timing-critical applications such as DSP and high-frequency processors. In contrast, the Vedic multiplier achieves lower dynamic power consumption and uses less hardware, due to its simplified and compact adder structure, making it more efficient for low-power and area-constrained VLSI systems.

Overall, the results show that there is no universal best multiplier—the optimal choice depends on the design goals. Applications prioritizing speed should opt for the Wallace Tree architecture, while those focused on power efficiency and compact layout benefit more from the Vedic multiplier.

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