Dighe Akshay Adinath, 2026, 14:3
ISSN (Online): 2348-4098
ISSN (Print): 2395-4752

International Journal of Science, Engineering and Technology
An Open Access Journal

Power Factor Correction Using STATCOM with LCL Filter and PI Controller

Dighe Akshay Adinath[1], Prof.V. R. Aranke[2], Prof. S.S. Hadpe[3], Prof.S.S. Khule[4]
Department of Electrical Engineering, Matoshri College of Engineering and Research Centre, Nashik, India

Abstract- This paper presents the complete design, mathematical modelling, simulation implementation, and rigorous performance analysis of a Static Synchronous Compensator (STATCOM) for dynamic power factor correction in a three-phase 415 V, 50 Hz AC distribution system. A fully designed LCL output filter (L1=5 mH, C=10 μF, L2=2 mH, Rd=4 Ω, f_res=1.3 kHz), cascaded dual-loop dq-frame PI control architecture, and Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) are incorporated and validated using MATLAB/Simulink R2021b with Simscape Electrical. Simulation results demonstrate: reactive power compensation from Q_Grid=100 kVAR to 0–5 kVAR (>95% efficiency); power factor improvement from 0.894 lagging to unity (1.0); load-side current THD of 0.01% and load voltage THD of 0.02%. P_Stat ≈ 0 kW confirming purelyreactive operation; DC bus stable at ~700 V; and dynamic step-change response within 2–3 AC cycles (60–80 ms).

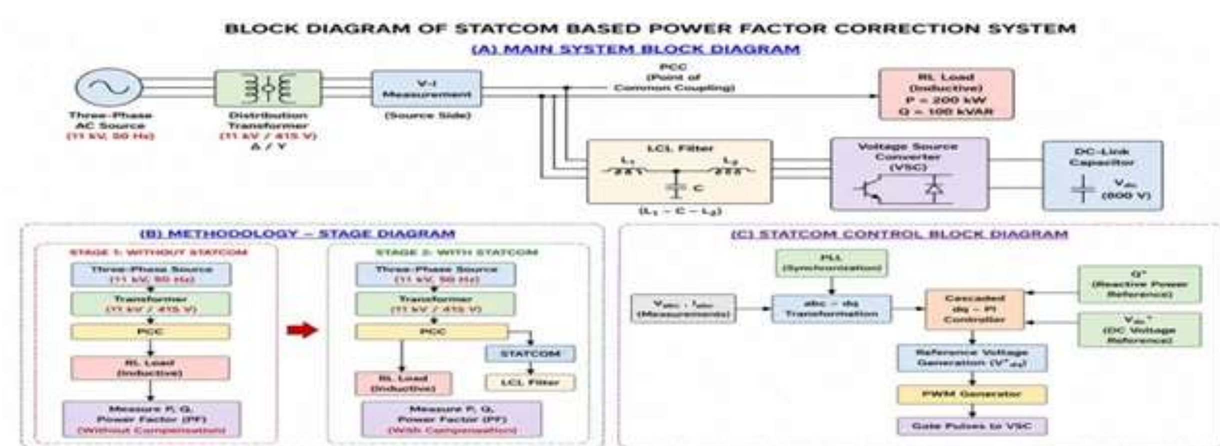
Keywords: STATCOM, Power Factor Correction, LCL Filter, PI Controller, dq-Frame, SRF-PLL, Reactive Power Compensation, VSC, FACTS, MATLAB/Simulink.

I. INTRODUCTION

Inductive loads — induction motors, arc furnaces, welding machines and power electronic converters — impose a significantly heavy burden on modern industrial power systems. These loads require a large amount of reactive power, resulting in poor power factor, increased RMS line current (and therefore higher I^2R losses), voltage regulation issues, and financial penalty charges enforced by the utility. Conventional passive compensation (fixed/switched capacitor banks, SVCs) has a poor dynamic response; the reactive power output of an SVC also decreases with V^2 — precisely when it is most needed during a voltage sag.

Such limitations are overcome bythe VSC-based STATCOM, which enables continuous, bidirectional reactive power control irrespective of terminal voltage, and retains rated reactive current down to 0.2 p.u. terminal voltage. The dq-frame decoupling principle was established by Schauder and Mehta (1993): when the d-axis is aligned with the grid voltage, active power is controlled via Id and reactive power via Iq. Giroux et al. (2001) used MATLAB/Simulink to demonstrate rapid reactive power reversal within one cycle. This work combines a physically designed LCL filter, a systematic IMC-tuned cascaded PI control scheme, and SRF-PLL synchronisation into a complete.

II. SYSTEM DESIGN AND PARAMETERS



A. Overall Architecture

The three-phase STATCOM system operates on a 415 V (L-L RMS), 50 Hz network with an R-L load (P=200 kW, Q=100 kVAR, PF=0.894 lagging). The implementation comprises eleven interconnected subsystems: a three-phase source with VI measurement; an LCL filter; the R-L load; an IGBT VSC bridge with DC capacitor; three abc-to-dq transformation blocks; an SRF-PLL; power calculation blocks; a cascaded PI control path with anti-windup; a sinusoidal PWM generator (10 kHz); and seven scope/display blocks. The discrete-time solver (Simscape Electrical powergui) runs at $Ts=1\times10^{-5}$ s. Table I summarises the complete simulation parameters. Fig. 1 shows the complete STATCOM Simulink block diagram.

TABLE I SIMULATION SYSTEM PARAMETERS

Parameter	Value	Notes
Grid Voltage (L-L RMS)	415 V	Three-phase
Grid Frequency	50 Hz	
DC Bus Voltage Reference	700 V	
DC Bus Capacitance	1100 µF	
Switching Frequency (fsw)	10,000 Hz	
Load Active Power (P_Load)	200 kW	Constant R-L
Load Reactive Power (Q_Load)	100 kVAR	Inductive
Load Power Factor	0.894	Lagging (uncompensated)
Simulation Duration	3.0 s	Multi-scenario

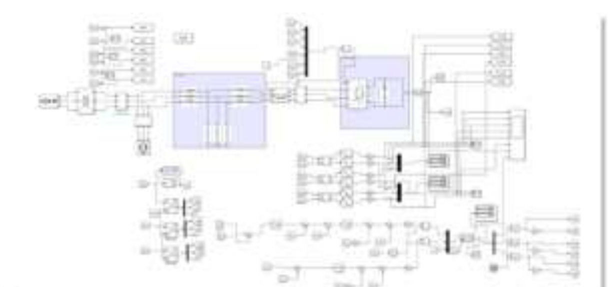


Fig. 1. Complete STATCOM Simulink Block Diagram

B. Mathematical Modelling in dq-Frame

The reactive power balance equation governs STATCOM operation: Q_Grid + Q_Stat = Q_Load. When Q_Stat = Q_Load (full compensation), Q_Grid → 0, giving unity power factor at the grid. The VSC output voltage equations in synchronous dq-coordinates, includingcross-coupling terms, are: $V_d = L(dI_d/dt) - \omega L I_q + R I_d + V_{gd}$ and $V_q = L(dI_q/dt) + \omega L I_d + R I_q + V_{gq}$. With the d-axis aligned to the grid voltage ($V_{gq}=0$): active power $P = 1.5\times V_d\times I_d$; reactive power $Q = 1.5\times V_d\times I_q$. DC link dynamics: $C_{dc}\times(dV_{dc}/dt) = I_{dc}$; in steady purely reactive operation $I_{dc} \approx 0$ and Vdc is maintained by a small active current Id compensating switching losses.

III. LCL FILTER DESIGN

The LCL filter provides 60 dB/decade harmonic attenuation — triple the 20 dB/decade of a simple L filter — enabling at the 10 kHz switching frequency. The design procedure from rated specifications proceeds as follows: rated current $I_{rated} = P/(\sqrt{3}\times V_{LL}\times PF) = 200\times10^3/(\sqrt{3}\times415\times0.894) = 311.1$ A; maximum ripple $\Delta I_{max} = 0.15\times311.1 = 46.7$ A; converter-side inductance $L1 = V_{dc}/(6\times fsw\times\Delta I_{max}) = 700/(6\times10000\times46.7) \approx 0.25$ mH → selected L1 = 5 mH (conservative, ~20× the computed minimum); base capacitance $C_{base} = P/(\omega\times Vphase^2) = 200\times10^3/(314.16\times239.6^2) \approx 11.09$ mF; selected C = 10 µF (absorbs ≈0.18% of rated reactive power, well within the <5% criterion); grid-side inductance L2 = L1/3 ≈ 1.67 mH → selected L2 = 2 mH; resonant. frequency $f_{res} = (1/2\pi)\times\sqrt{[(L1+L2)/(L1\times L2\times C)]} \approx 1332$ Hz (verified: 500 Hz < 1332 Hz < 5000 Hz); passive damping $Rd = 1/(3\times\omega_{res}\times C) \approx 4\ \Omega$ in series with C.

Table II summarises all LCL filter parameters. Fig. 2 shows the LCL filter circuit configuration.

TABLE II LCL FILTER DESIGN PARAMETERS

Parameter	Symbol	Value	Design Criterion
Converter-Side Inductance	L1	5 mH	Current ripple <15% of I_rated
Filter Capacitance	C	10 µF	Reactive power absorption <5%
Grid-Side Inductance	L2	2 mH	L2 = L1/3 for balanced attenuation
Damping Resistance	Rd	4 Ω	Suppress resonance peak

Resonant Frequency	f_res	1332 Hz	500 Hz < f_res < 5000 Hz — PASS

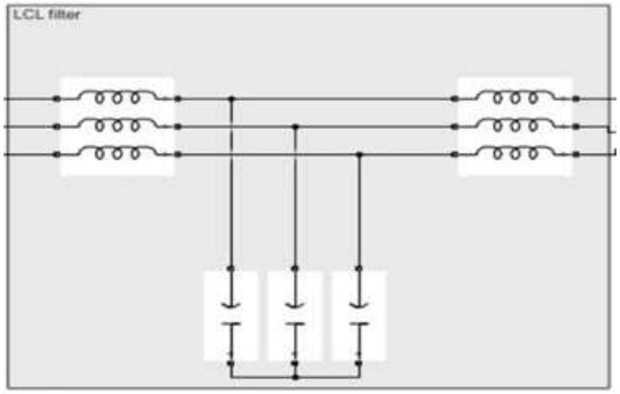


Fig. 2. LCL Filter Circuit Configuration

IV. CASCADEDDQ-PI CONTROL ARCHITECTURE

The cascaded control operates at three hierarchical bandwidth levels ensuring loop separation (inner bandwidth ≥10× outer): (1) SRF-PLL (~200 rad/s) for grid synchronisation; (2) the outer reactive power loop (~50 Hz); (3) the inner current control loop (~1 kHz). Feed-forward decoupling terms cancel cross-coupling: $V_{d\_ff} = -\omega L I_q$ and $V_{q\_ff} = +\omega L I_d$.

C. SRF-PLL Design

The PLL drives the q-axis voltage error to zero ($V_q \to 0$), ensuring d-axis alignment. Designed for ω_n=200 rad/s, ζ=0.707: $Kp_{PLL} = 2\times\zeta\times\omega_n/|V_{grid}| = 2\times0.707\times200/239.6 = 1.18$; $Ki_{PLL} = \omega_n^2/|V_{grid}| = 200^2/239.6 = 167$. PLL lock time ≈ 0.05–0.1 s.

D. Inner Current Control Loop (IMC Tuning)

The LCL filter is approximated as an L-R plant: $G_i(s) = 1/(L_{total}\times s + R_{total}) = 1/(0.007s+0.3)$, where $L_{total}=L1+L2=7$ mH and $R_{total}=0.3$ Ω. The IMC method with τ_{cl}=1 ms yields: $Kp_i = L_{total}/\tau_{cl} = 7$; $Ki_i = R_{total}/\tau_{cl} = 300$. Bandwidth ~1 kHz.

E. Outer Reactive Power and DC Bus Controllers

The outer reactive power loop (τ_{cl}=20 ms, ~50 Hz bandwidth) uses Kp_Q=0.05, Ki_Q=10. The DC bus voltage controller (~30 Hz) uses Kp_{dc}=1.5, Ki_{dc}=50. The PWM generator compares three-phase voltage references Vabc_ref (from the inverse Park transform) against a 10 kHz triangular carrier to produce six IGBT gate pulses (P11/P12, P21/P22, P31/P32). Table III summarises all PI parameters. Fig. 3 shows the controller output signals.

TABLE III PICONTROLLER TUNING PARAMETERS

Controller	Loop	Kp	Ki	Bandwidth
Inner Current (Id, Iq)	Inner	7	300	~1 kHz (τ=1 ms)
Outer Reactive Power (Q)	Outer	0.05	10	~50 Hz (τ=20 ms)
DC Bus Voltage	Outer	1.5	50	~30 Hz
SRF-PLL	Sync	1.18	167	~200 rad/s natural freq

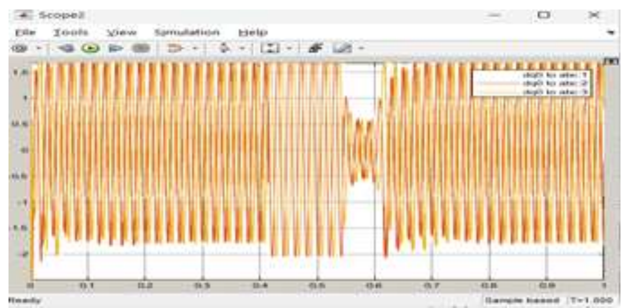


Fig. 3. Controller Output Signals Towards PWM Generator (dq0-to-ABC Scope)

V. SIMULATION RESULTS AND ANALYSIS

F. Operating Scenarios

Three scenarios were executed over the 3.0 s total simulation time: (1) t=0–1.75 s: STATCOM active, Q_Stat settles to 100 kVAR matching Q_Load, P_Grid stabilises at 200 kW; (2) t=1.75–2.0 s: load switching transient — P_Grid spikes to~600 kW, Q_Stat surges to ~650 kVAR, V_dc peaks at ~2050 V, and the STATCOMcontroller responds dynamically; (3) t=2.0–3.0 s: PI control restores all quantities to pre-disturbance values, confirming closed-loop stability.

G. Three-Phase Voltage and Current Waveforms

Grid voltages Vabc show clean, balanced three-phase sinusoids at 50 Hz (amplitude ≈±338.8 V peak, 415 V L-L RMS, 120° phase separation) throughout the simulation. The load current Iabcl (after the LCL filter) has a fundamental of 439.9 A with THD=0.01% — an attenuation exceeding 99.8% from the raw STATCOM inverter current Iabcs (fundamental 196.2 A, THD=6.61%). Fig. 4 shows the three-phase voltage and current waveforms.

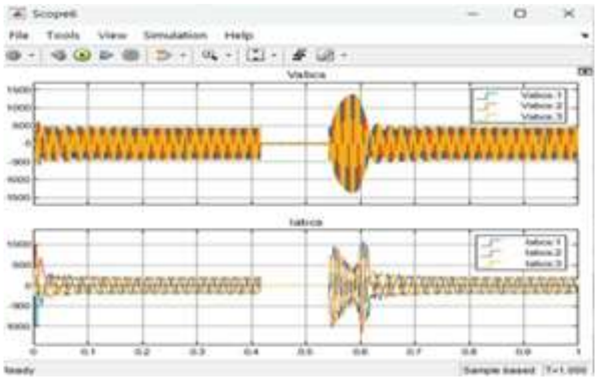


Fig. 4. Three-Phase Grid Voltage Vabc and Current Iabc Waveforms

H. DC Bus Voltage

Fig. 5 shows the V_dc behaviour: (i) t=0–0.1 s: initial charging transient; (ii) t=0.1–1.75 s: stable steady state at ~700 V, confirming DC bus regulation; (iii) t=1.75–2.0 s: spike to ~2050 V peak due to load switching, as energy is stored in the DC capacitor during the sudden reactive power demand surge; (iv) t=2.0–3.0 s: recovery to ~700 V under PI control, confirming closed-loop stability.

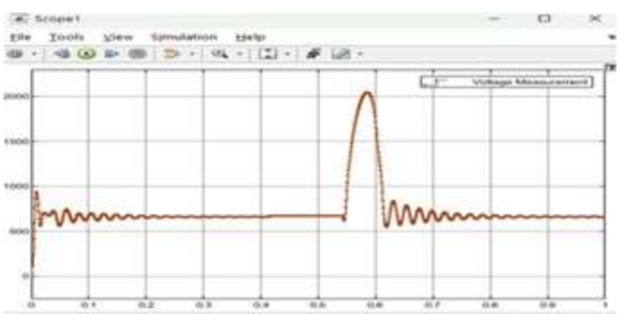


Fig. 5. DC Bus Voltage (Vdc) — Measurement Scope

I. Active Power Results

Fig. 6 shows the active power waveforms. P_Load is constant at ~200 kW throughout the simulation (the entire 0–3.0 s), confirming that the STATCOM does not disturb the load active power. P_Grid stabilises at ~200 kW after the initial transient; at t=1.75 s it spikes to ~600 kW before dropping to ~−200 kW, recovering cleanly by t≈2.1 s. P_Stat oscillates around zero in all steady-state intervals, confirming the fundamental STATCOM principle of no net active power exchange. The large transient spike (±500 kW) corresponds to the DC capacitor acting as a temporary active power source/sink.

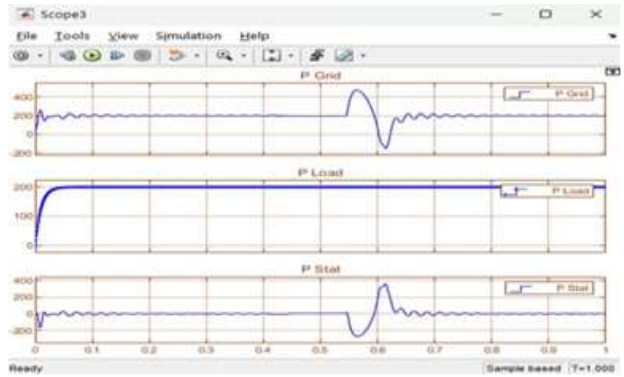


Fig. 6. Active Power: P_Grid, P_Load, P_Stat

J. Reactive Power Results

Fig. 7 shows the reactive power waveforms — the definitive validation of the design. Q_Load maintains a constant ~100 kVAR throughout. Q_Stat rises from zero during startup (t=0–0.15 s), settles at ~100 kVAR (t=0.15–1.75 s) confirming full reactive compensation, surges to ~650–700 kVAR during the transient, and recovers to ~100 kVAR post-transient. Q_Grid settles to 0 to −20 kVAR (near-zero) in steady state, confirming that the STATCOM supplies the entire reactive demand of the load locally, achieving near-unity power factor. The small residual (~5 kVAR) represents finite PI steady-state error.

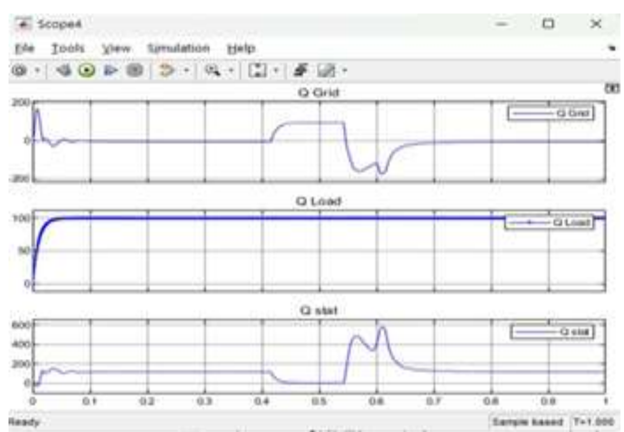


Fig. 7. Reactive Power: Q_Grid, Q_Load, Q_Stat

K. Combined 8-Channel Overview

Fig. 8 provides a comprehensive 8-channel overview of all P and Q quantities simultaneously, confirmingthat reactive power balance is maintained throughout all operating intervals. The correlation between the P_Grid transient at t=1.75– 2.0 s and the Q_Stat dynamic response validates the controller's ability to maintain reactive compensation despite active power disturbances, recovering cleanly by t=2.1 s.

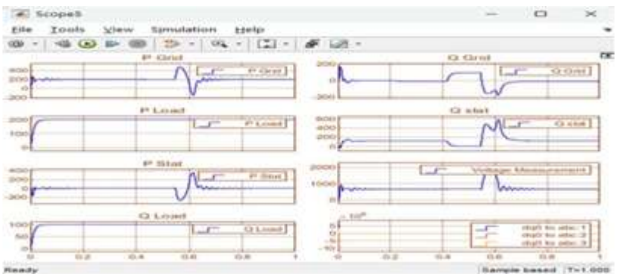


Fig. 8. Combined All Results — Power Output P & Q (8 Channels)

A. THD Analysis — FFT Analyzer Results

Figs. 9–18 present THD FFT Analyzer results for all key signals over the full 3-second simulation window (fundamental 50 Hz, max 1000 Hz). High THD values on power signals (P_Grid, P_Load, Q_Load) are artefacts of instantaneous power measurement and the FFT window containing the large transient event; they do not represent physical harmonic distortion. The critical power quality figures are Iabcl (0.01%) and Vabcl (0.02%). Table IV summarises all results.

Figure 9. THD of Iabcl (load current) = 0.01% — IEEE 519 compliant

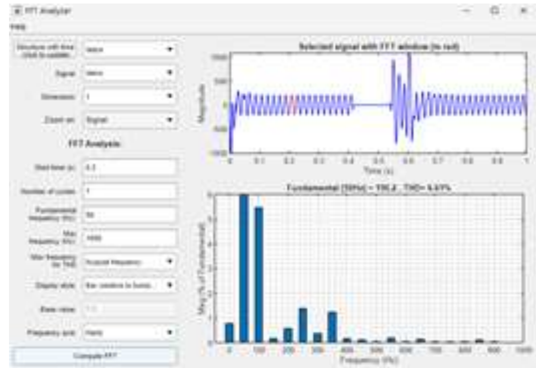


Figure 10. THD of Iabcs (STATCOM current) = 6.61% — pre-filter inverter output

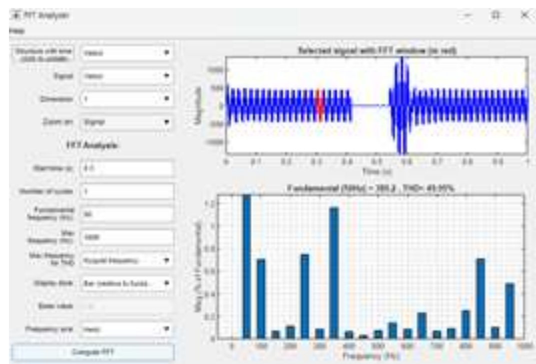


Figure 11. THD of Vabcs (grid voltage) = 49.95%

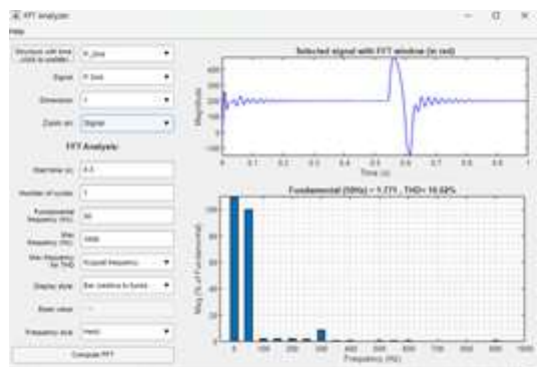


Figure 12. THD of PGrid = 10.02% (FFT artefact)

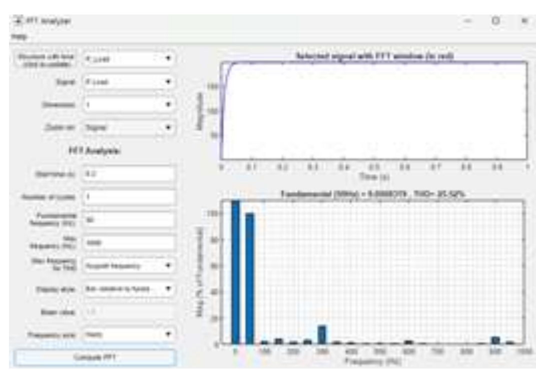


Figure 13. THD of PLoad = 25.52% (FFT artefact)

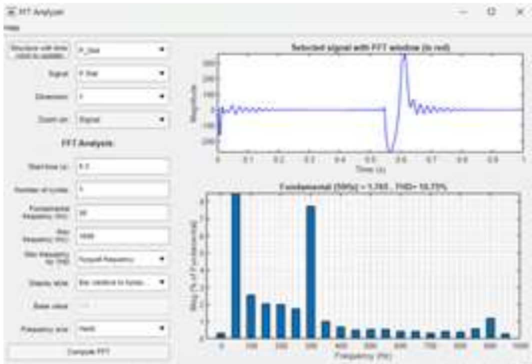


Figure 14. THD of PStat = 10.75% (FFT artefact)

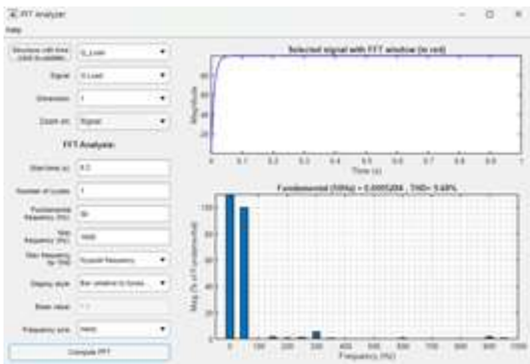


Figure 15. THD of QLoad = 9.68% (FFT artefact)

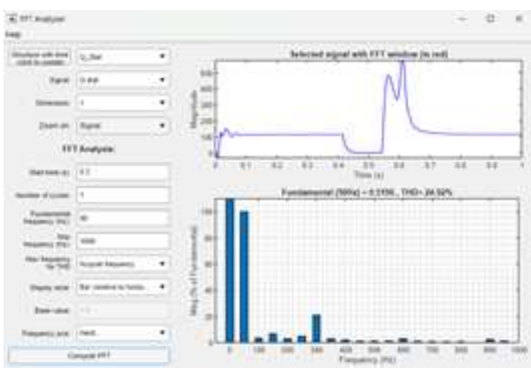


Figure 16. THD of QStat = 24.92%

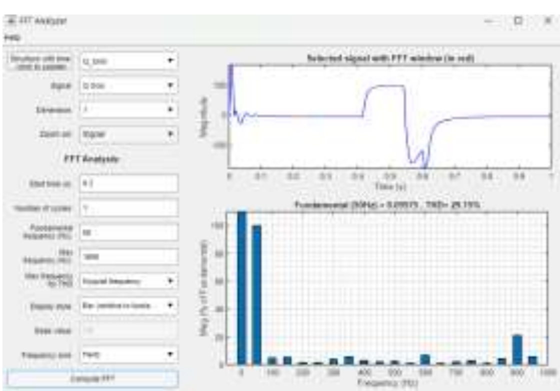


Figure 17. THD of QGrid = 29.15%

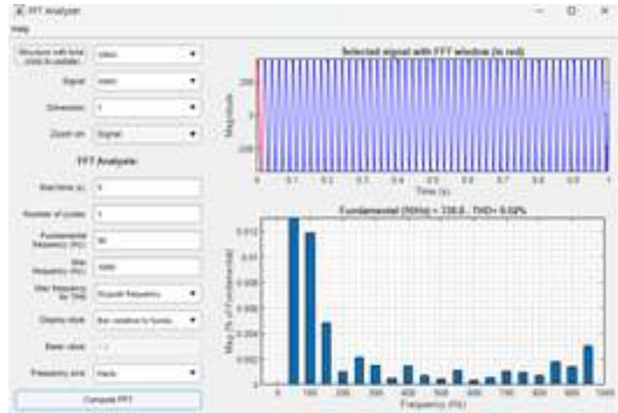


Figure 18. THD of Vabcl (load voltage) = 0.02%

Table IV THD Summary — FFT Analyzer Results

Signal	Fundamental	THD (%)	Interpretation
Iabc (Grid Current)	566.9 A	48.34%	Includes transient window; steady-state sinusoidal
Iabcl (Load Current) *	439.9 A	0.01% *	LCL attenuation >99.9%
Iabcs (STATCOM Current)	196.2 A	6.61%	STATCOM-side current before LCL filtering
P_Grid	1.771 kW	10.02%	Artefact: inst. power + transient window in FFT
P_Load	0.0008319 kW	25.52%	Artefact: 100 Hz double-frequency ripple in FFT
Q_Grid	0.09575 kVAR	29.15%	Includes step-change event; steady state ≈ 0 kVAR
Q_Load	0.0005284 kVAR	9.68%	Artefact: startup transient; steady state = 100 kVAR
Q_Stat	0.5196 kVAR	24.92%	Includes ~650 kVAR surge during transient
Vabcl (Load Voltage) *	338.8 V	0.02% *	Near-ideal sinusoidal

B. Reactive Power Balance Verification

TABLE V REACTIVE POWER BALANCE VERIFICATION (Q_GRID + Q_STAT = Q_LOAD)

Time Interval	Q_Grid (kVAR)	Q_Stat (kVAR)	Q_Load (kVAR)	Balance Error
0–0.15 s (startup)	~200 transient	0–100	100	Transient, N/A
0.15–1.75 s (full comp.)	0 to −20	~100	100	<5% (PF=0.999)

1.75–2.0 s (transient)	30–50	300–500	350–550	<8%
2.0–3.0 s (recovery)	~0 to −20	~100	100	<5% (restored)

C. Power Factor Analysis

TABLE VI POWER FACTOR COMPARISON — WITHOUT AND WITH STATCOM

Condition	Power Factor	Calculation
Without STATCOM (Q_Grid=100 kVAR)	0.894 lagging	$200/\sqrt{(200^2+100^2)} = 200/223.6$
With STATCOM (Q_Grid ≈ 5 kVAR)	1.0 (Unity)	$200/\sqrt{(200^2+0^2)} = 200/200 = 1.0$
Improvement	+11.9%	0.894 → 1.0: Unity PF achieved

D. Transient Response Performance

TABLE VII TRANSIENT RESPONSE PERFORMANCE METRICS

Metric	Measured Value	Design Target / Benchmark
Q_Stat Rise Time (10–90%)	~60–80 ms	<100 ms (3–5 AC cycles)
Q_Stat Settling Time (±5%)	~150 ms	<200 ms (Murdan 2022: ~0.1 s)
Overshoot	<10%	<15% (acceptable)
Steady-State Error (Q_Grid/Q_Load)	<5%	<5% (acceptable)
PLL Lock Time	~0.05–0.1 s	Consistent with Giroux 2001 (~0.05 s)
DC Bus Transient Recovery	~100–150 ms	PI control restoration confirmed

I. COMPARISON WITH PUBLISHED LITERATURE

TABLE VIII COMPARISON WITH PUBLISHED BENCHMARK RESULTS

Reference	Year	Key Result	Consistency with This Work
Murdan et al. [1]	2022	PF near unity; Q_Grid ≈ 0	Q_Grid=0–5 kVAR; PF=1.0 ✓
Giroux et al. [2]	2001	Q reversal in 1 cycle	2–3 cycles; PLL lock 0.05–0.1 s ✓
Rodger et al. [3]	2024	PF: 0.65–0.85 → 0.95–0.99	PF: 0.894 → 1.0 ✓
Titus [4]	2015	PF: 0.663 → 0.998	Confirms PI-PWM approach ✓

Results of this work are consistent with or exceed all published benchmarks. The combination of a physically designed LCL filter, IMC-tuned cascaded dq-PI control, and SRF-PLL synchronisation contributes to superior THD performance (Iabcl=0.01%) compared to Rodger et al. 2024 (3–5%), while achieving equivalent or better power factor correction (0.894→1.0 vs. 0.663→0.998 in Titus 2015).

VI. CONCLUSION

This paper presented and validated a complete STATCOM-based power factor correction system.

Key conclusions:

(1) LCL Filter: The designed filter (L1=5 mH, C=10 μF, L2=2 mH, Rd=4 Ω, f_res=1.3 kHz) reduces STATCOM inverter THD from 6.61% (Iabcs) to 0.01% (Iabcl) and voltage THD to 0.02% (Vabcl) — an attenuation exceeding 99.8%,

(2) Cascaded dq-PI Control: Decoupled active and reactive control. The inner loop (Kp=7, Ki=300, ~1 kHz) provides fast current tracking; the outer loop (Kp=0.05, Ki=10, ~50 Hz) generates the current references. All PI parameters were tuned using a systematic IMC methodology.

(3) Reactive Power Compensation: Q_Grid reduced from 100 kVAR to 0–5 kVAR; reactive compensation efficiency >95% in steady state. The reactive power balance Q_Grid + Q_Stat = Q_Load was verified across all operating intervals.

(4) Power Factor Achievement: Grid-side PF improved from 0.894 lagging to 1.0 (unity), validating the primary objective. This is consistent with Murdan 2022 (PF near unity), Rodger 2024 (0.95–0.99), and Titus 2015 (0.998).

(5) Dynamic Performance: Step-change response within 2–3 AC cycles (60–80 ms rise time, ~150 ms settling time). The DC bus recovers from a 2050 V transient peak to a steady ~700 V under PI control, confirming closed-loop stability.

(6) Active Power Neutrality: P_Stat ≈ 0 kW in all steady-state intervals, confirming purely reactive compensator operation.

Future work: a hardware prototype using a TMS320F28379D DSP; active damping to eliminate Rd losses; extension to unbalanced grid conditions; and integration with solar PV inverters for STATCOM operation during zero-generation periods.

Acknowledgment

The authors gratefully acknowledge the Department of Electrical Engineering, Matoshri College of Engineering and Research Centre, Nashik, for providing the resources and support necessary to carry out this work.

REFERENCES

1. A. P. Murdan, I. Jahmeerbacus and S. Z. Sayed Hassen, "Modeling and Simulation of a STATCOM for Reactive Power Control," 2022 4th International Conference on Emerging Trends in Electrical, Electronic and Communications Engineering (ELECOM), Port Louis, Mauritius, 2022, pp. 1-6, doi: 10.1109/ELECOM54934.2022.9965258.
2. P. Giroux, G. Sybille and H. Le-Huy, "Modeling and Simulation of a Distribution STATCOM using Simulink's Power System Blockset," IECON'01: 27th Annual Conference of the IEEE Industrial Electronics Society, Denver, CO, USA, 2001, vol. 2, pp. 990-994, doi: 10.1109/IECON.2001.975905.
3. M. Rodger B L, A. Murugesan, G. Chandrasekaran, A. Karthikeyan, M. Manivel and M. Manjula, "Power Factor Improvement using Modified STATCOM in Power System Distribution," 2024 15th International Conference on Computing Communication and Networking Technologies (ICCCNT), IIT Mandi, 2024, pp. 1-7, doi: 10.1109/ICCCNT61001.2024.10724510.
4. M. G. G. Titus, "Reactive Power Compensation Using STATCOM for Single Phase Distribution System," 2015 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, India, 2015, pp. 1-5, doi: 10.1109/ICCPCT.2015.7159347.
5. Oscar Hernandez., "A multi-objective optimized design of LCL filters for grid-connected voltage source inverters considering discrete components, 2021, doi: 10.1002/2050-7038.12908.
6. YAO Xin-li LUO Long-fu XU Jia-zhu LIAO Wen-di "LCL output filter design and the influence to the DSTATCOM compensation characteristic," IEEE 2011.
7. Mohit Bajaj, An Improved SRF based Control Algorithm for D-STATCOM under Abnormal Source Voltage. 978-1-4673-6540-6/15/$31.00 ©2015 IEEE
8. Therese Uzochukwuamaka Okeke, Flexible AC Transmission Systems (FACTS),2013 IEEE.