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High-Speed Low-Noise Dynamic Comparator for ADC Applications: Design and Simulation in 50 nm CMOS

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Abstract- High-speed and low-noise comparators are essential building blocks of modern analog-to-digital converters (ADCs), where propagation delay, noise, offset voltage, power consumption, and circuit complexity directly influence the overall conversion performance. This paper presents the design and simulation of a high-speed, low-noise dynamic CMOS comparator intended for high-performance analog and mixed-signal applications. A comparative analysis of conventional dynamic latch-based, double-tail latch-based sense-amplifier, uncalibrated dynamic, and reconfigurable dynamic comparator architectures is performed using key performance parameters including propagation delay, operating speed, RMS noise, offset voltage, slew rate, and transistor count. The proposed architecture incorporates a differential amplifier stage within the regenerative latch and employs optimized clocking to improve signal integrity and decision speed. The design is evaluated using LTspice IV with a 50 nm CMOS technology model. Simulation results indicate a minimum propagation delay of 0.650 ns, corresponding to a maximum operating speed of 1.538 GHz. The proposed comparator also achieves an RMS noise of 704.38 μV while using 13 transistors. The results demonstrate a balanced trade-off between speed, noise performance, and circuit complexity. The proposed architecture can therefore serve as a suitable comparator core for high-speed ADCs and other low-power mixed-signal systems.

Keywords— CMOS comparator, dynamic comparator, analog-to-digital converter, low-power VLSI, low-noise circuit, propagation delay, 50 nm CMOS, LTspice.

I. INTRODUCTION

The continuous development of wireless communication, biomedical instrumentation, Internet of Things (IoT), portable electronics, and high-speed data acquisition systems has increased the demand for high-speed and energy-efficient analog-to-digital converters. The comparator is one of the most important building blocks of an ADC because it determines the relative magnitude of two input signals and consequently influences conversion speed, accuracy, power consumption, and noise performance.

Dynamic comparators are widely investigated for high-speed ADC applications because regenerative feedback can provide rapid decision making while avoiding continuous static power consumption. However, increasing the operating speed often results in increased noise, offset, kickback effects, and power consumption. Thus, comparator design involves a significant trade-off among speed, power, accuracy, noise, and circuit complexity.

Previous research has investigated several dynamic comparator structures. Babayan-Mashhadi and Lotfi presented an analysis and design of a low-voltage, low-power double-tail comparator and demonstrated the importance of regeneration and delay optimization in dynamic comparator design [1]. Their work showed that modifying the regeneration mechanism can substantially improve comparator speed and power characteristics. Khorami and Sharifkhani subsequently presented a low-power high-speed comparator using controlled preamplification and latch activation, demonstrating the importance of timing optimization in achieving high-speed operation [2]. Other studies have also investigated offset, kickback noise, charge sharing,

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and common-mode limitations in dynamic comparators [3], [4].

Despite these developments, simultaneous optimization of propagation delay, RMS noise, offset, and circuit complexity remains challenging. The present research therefore investigates different dynamic comparator architectures and proposes an improved architecture aimed at achieving high speed and reduced noise without significantly increasing circuit complexity.

The major objectives of this research are:

- To study the operating principles of CMOS dynamic comparator architectures.
- To analyze conventional dynamic latch-based and double-tail comparator structures.
- To evaluate comparator performance in terms of delay, speed, RMS noise, offset voltage, slew rate, and transistor count.
- To design an improved dynamic comparator architecture.
- To evaluate the proposed architecture using LTspice IV.
- To investigate its suitability for high-speed ADC and mixed-signal applications.

The research methodology and simulation environment are based on the thesis study, which evaluates comparator architectures using deep-submicron CMOS technology and LTspice IV.

II. BACKGROUND AND RELATED WORK

1. Dynamic CMOS Comparators

A dynamic comparator generally operates in two principal phases: reset and evaluation. During the reset phase, internal nodes are initialized to predetermined voltage levels. During the evaluation phase, the differential input signal produces a voltage difference that is amplified by the regenerative latch.

The positive-feedback mechanism of the latch rapidly increases a small differential voltage into a full logic-level output. Consequently, the regeneration process strongly influences the propagation delay and operating frequency of the comparator. The block diagram of CMOS Comparator

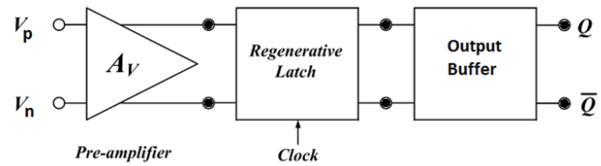

Figure 1: General type of CMOS Comparator

Dynamic comparators offer advantages such as high speed and low static power consumption. However, their performance can be affected by transistor mismatch, parasitic capacitance, charge sharing, clock feedthrough, kickback noise, and input offset.

2. Double-Tail Dynamic Comparator

The double-tail dynamic comparator separates the input amplification and regeneration functions through two tail devices. This structure is useful for low-voltage operation because it reduces transistor stacking and provides greater flexibility in controlling the preamplification and regeneration processes.

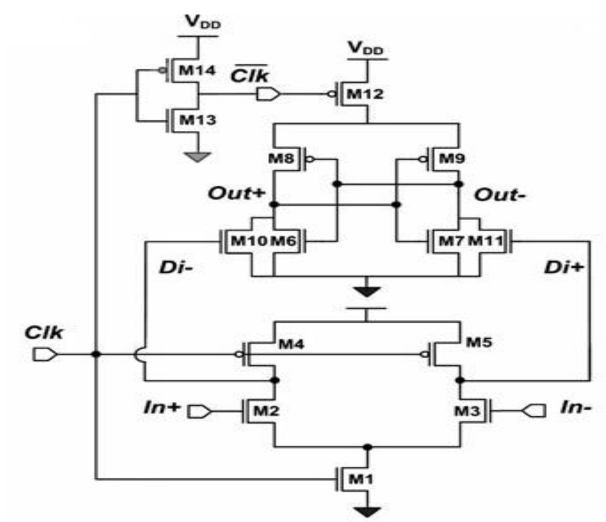

Figure 2: Double Tail latch type voltage sense amplifier

Babayan-Mashhadi and Lotfi demonstrated that appropriate modification of the double-tail structure can improve both delay and power characteristics at low supply voltages [1]. Their work established an important design direction for high-speed, low-power comparator architectures.

3. Low-Power High-Speed Comparator

Khorami and Sharifkhani proposed a comparator employing controlled preamplification and delayed latch activation. Their work demonstrated that proper timing between amplification and regeneration can improve speed while controlling power consumption [2]. The reported design was validated using process-voltage-temperature analysis, Monte Carlo simulation, and silicon measurements.

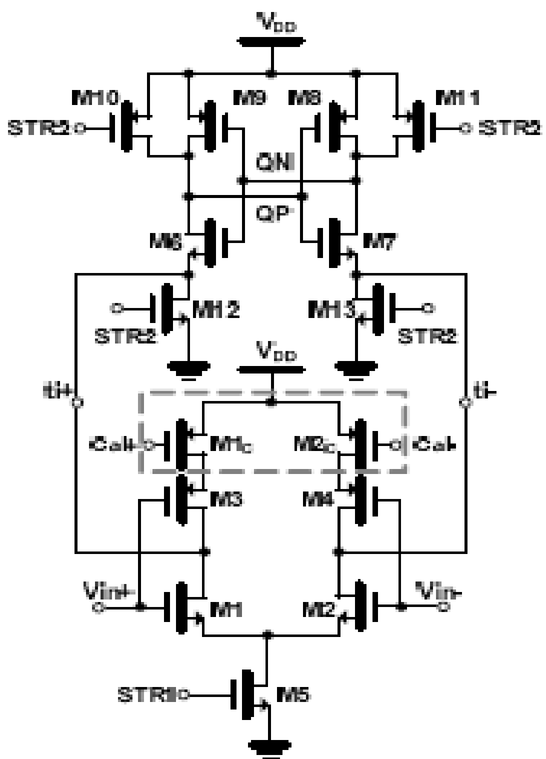

Figure 3: Reconfigurable Dynamic CMOS Comparator

These developments indicate that comparator performance depends not only on transistor topology but also on regeneration timing, transistor sizing, parasitic capacitance, and input signal conditions.

III. COMPARATOR ARCHITECTURES AND RESEARCH METHODOLOGY

1. Comparative Architectures

Four conventional comparator architectures were considered in the study:

- Dynamic latch-based comparator.
- Double-tail latch-based sense-amplifier comparator.
- Dynamic comparator without calibration.
- Reconfigurable dynamic CMOS comparator.

These architectures were evaluated using propagation delay, operating speed, offset voltage, slew rate, RMS noise, and transistor count. The comparative analysis demonstrated that each architecture exhibits different trade-offs between speed, noise, and complexity.

2. Simulation Environment

LTspice IV was used as the primary simulation environment. The research considered CMOS technology nodes including 45 nm, 65 nm, and 50 nm during the design and comparative study, with the proposed architecture evaluated using a 50 nm CMOS technology model.

The principal performance parameters investigated were:

- Propagation delay
- Operating frequency
- RMS noise
- Offset voltage
- Slew rate
- Power consumption
- Transistor count

The simulation methodology was designed to provide a comparative evaluation of the proposed architecture against conventional dynamic comparator structures.

IV. PROPOSED DYNAMIC COMPARATOR

The proposed architecture is developed to address the principal limitations observed in conventional dynamic comparators. The architecture incorporates a differential amplifier stage within the latch structure to improve input signal discrimination and noise suppression.

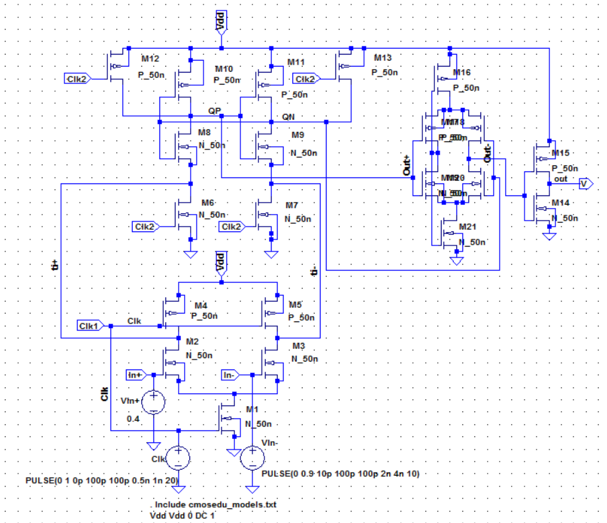

Figure 4: Proposed dynamic comparator circuit

The differential input stage generates a voltage difference corresponding to the input signals. This differential signal is subsequently amplified through the regenerative latch. The positive feedback mechanism accelerates the decision process and enables rapid transition of the output toward the corresponding logic state.

An optimized clocking arrangement is also incorporated to control the timing of the comparator stages. Proper clock control helps coordinate signal amplification and regeneration and contributes to improved timing performance.

The design therefore focuses on three major objectives:

- reduction of propagation delay,
- improvement of noise performance, and
- maintenance of reasonable circuit complexity.

The thesis describes the proposed architecture as a dynamic comparator incorporating a differential amplifier stage within the latch and optimized clocking techniques for improved speed and signal integrity.

V. PERFORMANCE ANALYSIS

1. Propagation Delay

Propagation delay represents the time required for the comparator output to respond to a differential input condition. It is one of the most important parameters in high-speed ADC applications.

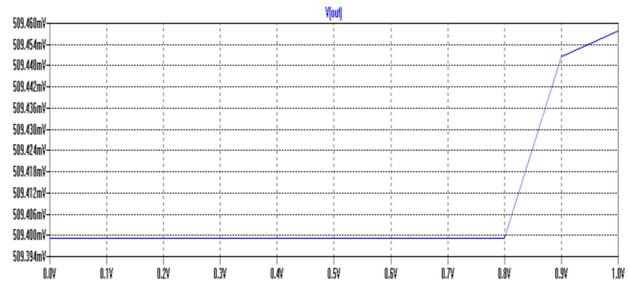

Figure 5: DC Response of proposed comparator

The proposed comparator achieves a minimum simulated propagation delay of:

Tpd=0.650 nsT_{pd}=0.650\;ns

This reduced delay enables rapid comparator decision making and contributes directly to the high operating frequency of the proposed architecture.

2. Operating Speed

The maximum operating speed corresponding to the reported propagation delay is:

fmax=1.538 GHzf_{max}=1.538\;GHz

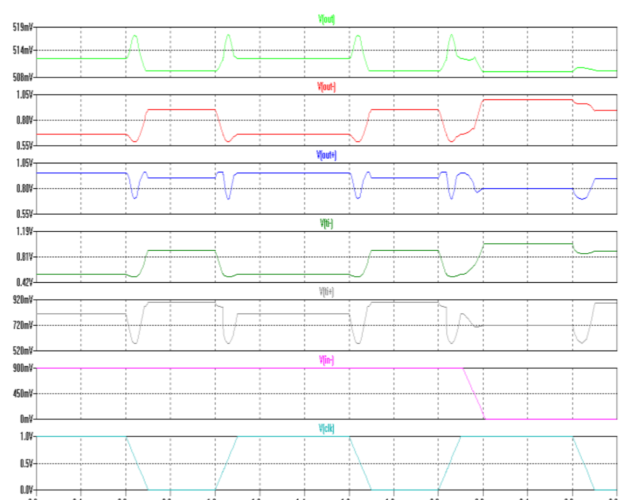

Figure 6: Transient response of proposed comparator

The proposed architecture therefore demonstrates high-speed operation appropriate for high-frequency mixed-signal and ADC applications.

3. RMS Noise

Noise is an important consideration in precision analog and mixed-signal circuits because excessive noise can result in incorrect comparator decisions.

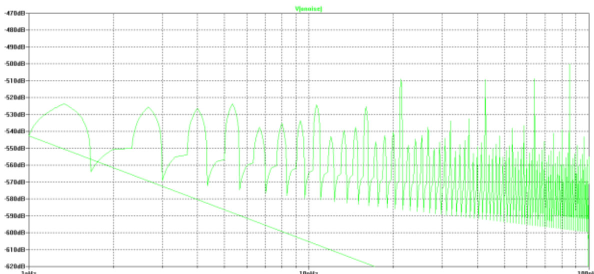

Figure 7: Noise spectrum of proposed comparator

The proposed architecture achieves an RMS noise of: Vn,RMS=704.38 µVV_{n,RMS}=704.38\;\mu V

The thesis attributes the improved noise performance to improved isolation between input and internal nodes, reduced charge-sharing effects, and optimized regenerative timing.

4. Offset Voltage

The simulated offset voltage reported for the proposed architecture is approximately:

VOS=509.399 mVV_{OS}=509.399\;mV

The offset performance remains an important area for further improvement, particularly for high-resolution ADC applications. The thesis therefore recommends the investigation of auto-zeroing, digital calibration, and offset-cancellation techniques in future work.

5. Slew Rate

The slew rate indicates the rate at which the comparator output changes between logic levels. The proposed comparator has a reported slew rate of approximately 0.0449 mV/ns. Although this value is lower than that of the reconfigurable comparator investigated in the study, the controlled transition contributes to stable switching behavior.

6. Transistor Count

The proposed architecture uses 13 transistors. This represents a moderate level of circuit complexity relative to the conventional architectures considered in the study. The design therefore provides a balance between circuit implementation complexity and performance.

VI. COMPARATIVE RESULTS

Table 1: Performance Summary of the Proposed Comparator

Parameter	Proposed Comparator
Technology	50 nm CMOS
Simulation Tool	LTspice IV
Propagation Delay	0.650 ns
Maximum Operating Speed	1.538 GHz
RMS Noise	704.38 µV
Offset Voltage	≈509.399 mV
Slew Rate	0.0449 mV/ns
Transistor Count	13

The reported results indicate that the proposed architecture provides a balanced combination of high operating speed, low propagation delay, reduced RMS noise, and moderate transistor count.
The comparative study further indicates that the conventional architectures involve different performance trade-offs. The double-tail architecture provides improved noise characteristics but may introduce additional delay, whereas an uncalibrated dynamic architecture can provide higher speed with increased sensitivity to noise and offset. The reconfigurable architecture provides a different balance between speed and noise but introduces additional clocking considerations.

VII. DISCUSSION

The results demonstrate that dynamic comparator performance cannot be optimized effectively using a single parameter. High operating speed generally requires rapid regeneration, whereas noise reduction may require controlled switching and improved isolation. Similarly, reduction in transistor count can reduce circuit complexity but may limit the flexibility available for offset and noise optimization.

The proposed architecture addresses these trade-offs through the combined use of differential amplification and regenerative feedback. The achieved propagation delay of 0.650 ns corresponds to an operating speed of 1.538 GHz, while the RMS noise is reduced to 704.38 μV. The 13-transistor implementation also maintains moderate circuit complexity.

The results are consistent with the broader research direction in dynamic comparator design, where regeneration timing, preamplification, offset, and noise are important determinants of performance. Existing studies have similarly emphasized the relationship between delay, power, offset, and noise in high-speed dynamic comparators [1]–[4].

However, the present results are simulation-based. Therefore, post-layout parasitic extraction, Monte Carlo analysis, PVT analysis, and silicon-level measurements would be required to establish practical robustness.

Applications

The proposed comparator can potentially be applied as a decision-making element in high-speed analog-to-digital conversion systems. Dynamic comparators are relevant to architectures such as Flash ADCs, SAR ADCs, and pipelined ADCs.

The low propagation delay makes the architecture relevant to high-speed conversion systems, while its reduced RMS noise may be beneficial in applications requiring improved signal discrimination.

Potential application areas include:

- High-speed ADCs
- SAR ADCs
- Flash ADCs
- Pipelined ADCs
- Wireless communication systems
- High-speed data acquisition
- Biomedical instrumentation
- IoT sensor interfaces
- Portable mixed-signal systems

The thesis specifically identifies Flash, SAR, and pipelined ADC integration as important directions for further evaluation of the proposed comparator.

Limitations and Future Work

Although the proposed comparator demonstrates improved simulated speed and noise characteristics, several areas require further investigation.

First, power optimization should be performed using techniques such as power gating, adaptive biasing, and charge recycling. Second, offset voltage can be further reduced using auto-zeroing and digital calibration.

The present architecture also uses dual-clock operation. Therefore, future work should investigate single-clock or self-timed architectures to minimize clock-skew-related limitations.

Further investigation should also include:

- Scaling the architecture to advanced CMOS technology nodes.
- Detailed Monte Carlo simulation.
- Process-voltage-temperature analysis.
- Post-layout simulation including parasitic effects.
- Offset-cancellation and calibration.
- Integration with complete ADC architectures.
- Experimental fabrication and silicon validation.
- Machine-learning-based transistor sizing and optimization.

The thesis identifies advanced technology scaling, adaptive calibration, PVT robustness, ADC integration, Monte Carlo analysis, and machine-learning-based optimization as important future research directions.

VIII. CONCLUSION

This paper presented the design and simulation of a high-speed, low-noise dynamic CMOS comparator for ADC applications. Four conventional dynamic comparator architectures were comparatively investigated with respect to propagation delay, operating speed, RMS noise, offset voltage, slew rate, and transistor count.

The proposed architecture incorporates a differential amplifier stage within the regenerative latch together with optimized clocking techniques. Simulation using a 50 nm CMOS technology model in LTspice IV demonstrates a minimum propagation delay of 0.650 ns and a corresponding maximum operating speed of 1.538 GHz. The architecture also achieves an RMS noise of 704.38 μV and uses 13 transistors.

The results demonstrate that the proposed comparator provides a balanced combination of speed, noise performance, and circuit complexity. The study also confirms that dynamic comparator design involves important trade-offs among delay, noise, offset, slew rate, power, and implementation complexity.

For practical deployment, further research is recommended in the areas of offset cancellation, power optimization, clocking, PVT robustness, Monte Carlo analysis, post-layout verification, advanced technology scaling, and complete ADC integration. These investigations can extend the proposed architecture toward next-generation high-speed and low-power mixed-signal systems.

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