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# Password-Based Digital Lock With 3-Attempts Security Using Verilog HDL

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**Abstract- The Password-Based Digital Lock with 3-Attempt Security Using Verilog HDL is a digital security system designed to provide controlled access through password authentication. The system is implemented using Verilog Hardware Description Language (HDL) and can be programmed on an FPGA board. The user enters a predefined password using input switches or a keypad. The entered password is compared with the stored password using digital logic. If the password matches, the system grants access by activating an unlock signal. If an incorrect password is entered, the system allows the user to retry up to three times. After three consecutive incorrect attempts, the system automatically locks the access and activates a security alert signal. A reset mechanism can be used to restore the system to its initial state. The design uses finite state machine (FSM) concepts, counters, comparators, and sequential logic. This project demonstrates the practical application of Verilog HDL in developing reliable, efficient, and secure digital access control systems.**

**Keywords— Password Authentication, Digital Lock, Verilog HDL, FPGA, Three-Attempt Security, Finite State Machine (FSM), Password Verification, Access Control, Digital Security, Counter.**

## I. INTRODUCTION

Security plays an important role in modern electronic systems, particularly in protecting personal belongings, confidential information, restricted areas, and valuable resources. Traditional mechanical locking systems use physical keys for access control. However, these systems have several limitations, such as the possibility of losing keys, unauthorized duplication, and misuse. To overcome these problems, digital locking systems provide a more secure, convenient, and reliable method of controlling access. A password-based digital lock is an electronic security system that allows authorized users to gain access by entering a predefined password.

The Password-Based Digital Lock with 3-Attempt Security Using Verilog HDL is designed to provide secure access through password authentication and a limited number of incorrect attempts. The system is developed using Verilog Hardware Description Language (HDL), which is widely used for designing and implementing digital circuits. The proposed system can be implemented on a Field Programmable Gate Array (FPGA) board, which allows the digital logic to be tested and verified in real time.

The basic working principle of the system is based on comparing the password entered by the user with a predefined password stored in the digital logic. The user enters the password using input switches or a keypad connected to the FPGA board. The system checks whether the entered password matches the stored password. If both passwords are identical, the system generates an unlock signal and grants access to the authorized user. An LED or another output device can be used to indicate the unlocked condition.

If the user enters an incorrect password, the system increases the attempt counter by one and allows the user to try again. The system provides a maximum of three attempts to enter the correct password. After three consecutive incorrect password entries, the system automatically enters a locked state. In this condition, further password entries are restricted, and a security alert can be activated using an LED or buzzer. This feature helps prevent unauthorized access through repeated password guessing.

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The proposed design uses various digital electronic concepts, including comparators, counters, registers, logic gates, sequential circuits, and Finite State Machines (FSM). The FSM controls different operating conditions of the system, such as the initial state, password entry, password verification, successful authentication, incorrect password detection, and security lockout. The counter maintains the number of incorrect attempts and controls the transition to the security lockout state.

Verilog HDL is used to describe the hardware functionality and implement the required digital logic. Simulation tools such as ModelSim or Xilinx Vivado can be used to verify the design before implementing it on FPGA hardware. The simulation helps identify logical errors and confirms that the system operates correctly under different password conditions.

The main objective of this project is to develop a simple, efficient, and cost-effective digital security system with an additional protection mechanism against repeated incorrect password attempts. The system can be used in electronic lockers, security cabinets, restricted rooms, small storage units, and other access control applications.

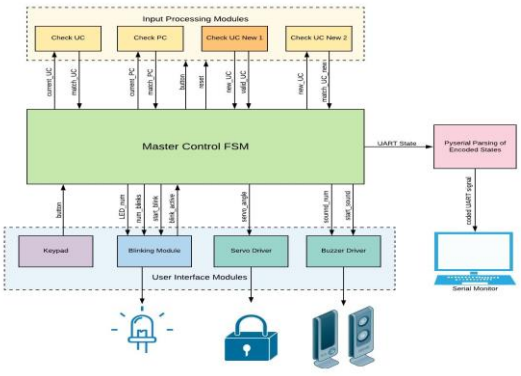
Overall, this project demonstrates the practical application of Verilog HDL, FPGA technology, and digital logic design in developing an electronic password authentication system. It provides a basic understanding of hardware-based security systems and creates opportunities for future improvements, such as password modification, LCD display integration, keypad interfacing, and advanced security features.

## II. WORKING

The Password-Based Digital Lock with 3-Attempt Security Using Verilog HDL works on the principle of password authentication and digital access control. The system verifies the password entered by the user and grants access only when the entered password matches the predefined password stored in the Verilog program. The complete operation is controlled using digital logic circuits and a Finite State Machine (FSM).

**Step-by-step Working**

- **System Initialization:** When the FPGA board is powered ON or reset, the system enters its initial state. The attempt counter is set to zero, and the lock remains in the locked condition.
- **Password Entry:** The user enters a predefined password using input switches or a keypad connected to the FPGA board.
- **Password Comparison:** The entered password is compared with the stored password using a comparator circuit implemented in Verilog HDL.
- **Correct Password:** If the entered password matches the stored password, the system generates an unlock signal. The access indicator LED turns ON, indicating successful authentication.
- **Incorrect Password:** If the entered password does not match, the system considers it an incorrect attempt and increments the attempt counter by one.
- **Second Attempt:** The user gets another opportunity to enter the correct password. If the password is still incorrect, the counter increases again.
- **Third Attempt:** The system allows a maximum of three incorrect password attempts. After the third incorrect attempt, the system automatically enters the security lockout state.
- **Security Alert:** In the lockout state, further password entries are disabled, and a buzzer or warning LED can be activated to indicate unauthorized access.
- **Reset Operation:** The reset button is used to initialize the system again, clear the attempt counter, and restore the normal locked condition.



**Advantages**

- Provides secure access through password authentication.
- Allows only authorized users to unlock the system.
- Limits password entry to three incorrect attempts.
- Prevents repeated unauthorized access attempts.
- Automatically activates a security alert after three wrong attempts.
- Uses FPGA technology for fast operation.
- Verilog HDL makes the design easy to modify and upgrade.
- Reduces dependency on traditional mechanical keys.
- Provides reliable and efficient digital security.
- Can be used in lockers, cabinets, doors, and restricted areas.
- Disadvantages:
- Requires a stable power supply to operate.
- Password can be forgotten by the authorized user.
- Limited to only three incorrect password attempts.
- Resetting may be required after system lockout.
- FPGA development boards can be expensive.
- Password may be exposed if shared with others.
- Hardware connections and programming errors may affect operation.
- Basic password systems may be vulnerable to password guessing.
- Requires proper hardware configuration and maintenance.
- Additional features increase system complexity and cost.

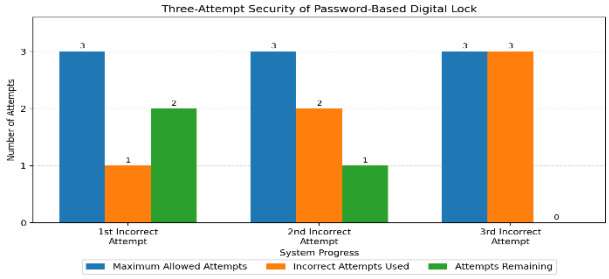



Chart -1: Performance Analysis of Three-Attempt Security in Password-Based Digital Lock Using Verilog HDL

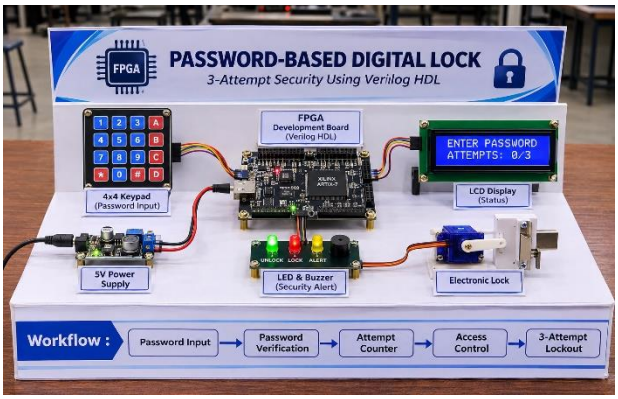



Figure 1: Prototype Model of Password-Based Digital Lock with Three-Attempt Security Using Verilog HDL on FPGA.

## III. CONCLUSION

The Password-Based Digital Lock with 3-Attempt Security Using Verilog HDL provides a simple, reliable, and efficient electronic security solution. The system verifies user passwords and grants access only when the correct password is entered. After three consecutive incorrect attempts, it automatically locks the system and activates a security alert. This project demonstrates the practical application of Verilog HDL, FPGA, counters, comparators, and Finite State Machines (FSM). It can be further improved by adding password change functionality, LCD display, and advanced security features for better protection.

## REFERENCES

1. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.
2. M. M. Mano and M. D. Ciletti, Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog, 6th ed. Pearson Education, 2018.
3. P. D. Minns and I. Elliott, FSM-Based Digital Design Using Verilog HDL. Chichester, U.K.: Wiley, 2008.
4. M. D. Ciletti, Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL. Upper Saddle River, NJ, USA: Prentice Hall, 2010.
5. IEEE, IEEE Standard for Verilog Hardware Description Language, IEEE Std 1364-2005, 2005.

6. S. Brown and Z. Vranesic, Fundamentals of Digital Logic with Verilog Design, 3rd ed. New York, NY, USA: McGraw-Hill, 2008.
7. Xilinx, Vivado Design Suite User Guide: Synthesis, UG901. San Jose, CA, USA: Xilinx.
8. Xilinx, 7 Series FPGAs Configuration User Guide, UG470. San Jose, CA, USA: Xilinx.