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Morse Code Generator Using FPGA

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Abstract- The Morse Code Generator Using FPGA is a digital communication system designed to convert input characters into their corresponding Morse code signals. Morse code represents letters, numbers, and special characters using short signals called dots (.) and long signals called dashes (-). The proposed system is implemented using a Field Programmable Gate Array (FPGA) and Verilog Hardware Description Language (HDL). Input characters are provided through switches or push buttons connected to the FPGA board. The system processes the input and generates the corresponding Morse code sequence using digital logic circuits. A clock divider and counter are used to maintain accurate timing for dot and dash signals. The generated Morse code output is displayed through an LED or buzzer, allowing users to identify the encoded message. The design uses important digital electronics concepts such as counters, registers, sequential circuits, and Finite State Machines (FSM). This project provides a practical understanding of FPGA programming, digital communication, and hardware design. It can be further enhanced by supporting multiple characters, LCD displays, and wireless communication.

Keywords— Morse Code, FPGA, Verilog HDL, Digital Communication, Dot and Dash, Clock Divider, Counter, Finite State Machine (FSM), LED Indicator, Sequential Circuits, VLSI Design.

I. INTRODUCTION

Communication is one of the most important aspects of human life. It allows people to share information, ideas, and messages over short and long distances. With the development of technology, different communication methods have been introduced to make information transmission faster, easier, and more reliable. One of the oldest and simplest methods of communication is Morse Code. It is a communication technique in which letters, numbers, and special characters are represented using a combination of short and long signals called dots (.) and dashes (-).

Morse code was developed by Samuel Morse and was widely used in telegraph communication. Earlier, it played an important role in transmitting messages through electrical signals over long distances. It was also used in ships, aircraft, military communication, and emergency signaling systems. Even today, Morse code is considered a useful communication technique because it is simple, requires less bandwidth, and can be transmitted using different types of signals such as sound, light, and radio waves.

The Morse Code Generator Using FPGA is a digital electronics project designed to automatically convert input characters into their corresponding Morse code signals. The main purpose of this project is to generate Morse code using an FPGA (Field Programmable Gate Array). An FPGA is a programmable semiconductor device that can be configured to perform different digital logic operations. Unlike fixed-function digital circuits, an FPGA can be reprogrammed according to the requirements of an application. It provides flexibility, fast processing, and efficient hardware implementation.

In this project, Verilog Hardware Description Language (HDL) is used to design and implement the Morse code generator. Verilog is a hardware description language commonly used in VLSI and digital system design. It helps describe the behavior and structure of digital circuits. Using Verilog, different functional blocks such as input units, encoders, counters, clock dividers, and control units can be designed and implemented on an FPGA development board.

The system accepts input characters through switches or push buttons connected to the FPGA

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board. When the user selects a particular character, the FPGA receives the input and processes it using the programmed logic. The corresponding Morse code pattern is selected from the predefined encoding logic. The system then converts the encoded pattern into a sequence of short and long output signals.

In Morse code, a dot represents a short signal, while a dash represents a long signal. The duration of these signals is an important part of Morse code generation. Therefore, a clock divider circuit is used to reduce the high-frequency clock signal of the FPGA and generate suitable timing intervals. Counters are used to control the duration of each signal, while a control unit manages the sequence of dots, dashes, and gaps between them.

The generated Morse code can be represented using an LED or buzzer connected to the FPGA output. When a dot is generated, the LED glows for a short duration or the buzzer produces a short sound. Similarly, when a dash is generated, the LED remains ON for a longer duration or the buzzer produces a long sound. In this way, the user can easily identify the generated Morse code through visual or audio signals.

II. WORKING

The Morse Code Generator using FPGA is a digital electronic system designed to convert input characters into their corresponding Morse code signals. The system works with the help of an FPGA (Field Programmable Gate Array), which is programmed using Verilog HDL. Initially, the user enters an alphabet or character through input switches or a keypad connected to the FPGA board. The entered character is received by the FPGA in binary form. The input section provides the character data to the internal processing unit of the FPGA, where the programmed logic identifies the entered character.

After receiving the input, the character-to-Morse code conversion unit converts the selected alphabet into its corresponding Morse code pattern. Each alphabet and number has a unique combination of dots (.) and dashes (–). A dot represents a short-duration signal, whereas a dash represents a long-duration signal. The conversion process is performed using predefined logic or a lookup table written in Verilog HDL. The FPGA checks the input character and selects the appropriate Morse code sequence from the stored patterns. For example, the alphabet 'A' is represented by .-, the alphabet 'B' by -..., and the alphabet 'C' by -.-..

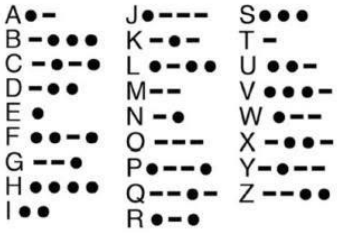
Once the Morse code pattern is generated, the timing control unit controls the duration of each dot, dash and gap between the signals. The FPGA clock is used to generate accurate timing pulses. A clock divider circuit reduces the clock frequency to obtain the required timing intervals. The short-duration pulse is generated for a dot, while a longer-duration pulse is generated for a dash. Proper gaps are also provided between dots and dashes to distinguish the individual signals clearly.

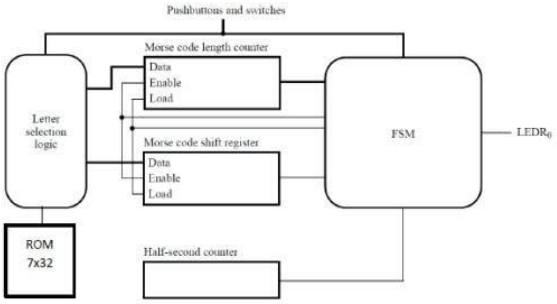
After timing control, the generated Morse code is sent to the output section. An LED or buzzer is connected to the FPGA board to represent the Morse code signals. When the output signal is HIGH, the LED glows or the buzzer produces sound. When the output signal is LOW, the LED turns OFF or the buzzer stops producing sound. In this way, short and long signals are generated according to the selected Morse code pattern. For example, when the user enters the letter 'A', the FPGA generates two signals: first a short signal (dot) followed by a long signal (dash), with a proper time gap between them.

The system continues generating the Morse code until the complete sequence for the entered character is transmitted. After completing the operation, the system can wait for the next input character. A reset facility can also be provided to clear the previous data and initialize the system for a new operation. The entire process is controlled by the Verilog program implemented inside the FPGA, which performs input processing, character conversion, timing generation and output control.

Thus, the Morse Code Generator using FPGA provides an efficient method of converting digital input characters into understandable Morse code

signals. This project demonstrates the practical application of FPGA technology, Verilog HDL programming, digital logic design, clock division and signal generation. It can be used for educational purposes, emergency signalling, optical communication and basic digital communication applications.





Advantages

- High-speed operation provides fast Morse code generation.
- High accuracy ensures correct dot and dash signals.
- Reprogrammability allows easy modification of the system.
- Low power consumption reduces energy requirements.
- Reliable operation provides consistent output signals.
- Real-time processing converts characters quickly.
- Flexible output supports LED and buzzer devices.
- Compact design reduces hardware requirements.
- Easy modification is possible through Verilog programming.
- Future expansion allows additional characters and features.

Disadvantages

- High hardware cost increases the initial investment.
- Complex programming requires knowledge of Verilog HDL.
- Limited input options may restrict character entry.
- External components are required for output generation.
- Power supply is necessary for continuous operation.
- Limited communication range affects signal transmission.
- Debugging errors in hardware and software can be difficult.
- FPGA development requires technical knowledge and experience.
- Hardware dependency makes the system dependent on the FPGA board.
- Limited memory may restrict the storage of additional Morse code patterns.

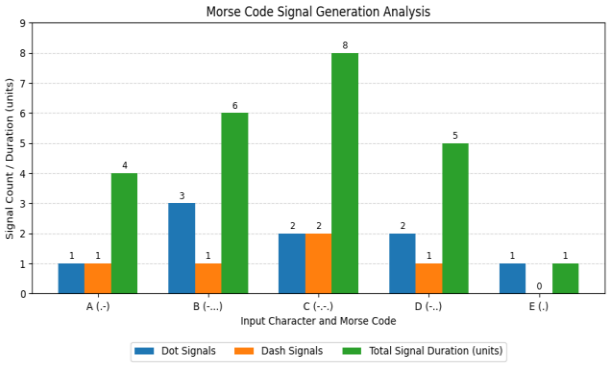


Chart -1 Morse Code Signal Analysis

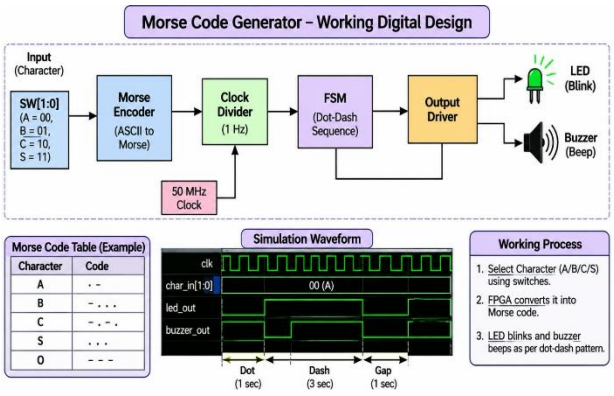


Figure 1: Block Diagram and Simulation Waveform of Morse Code Generator Using FPGA.

III. CONCLUSION

The Morse Code Generator Using FPGA is an efficient digital communication system that converts input characters into their corresponding Morse code signals using dots and dashes. The system is implemented using Verilog HDL and FPGA technology. It provides accurate timing, fast processing and reliable output through an LED or buzzer. This project helps in understanding digital logic design, FPGA programming and signal generation. It can be useful in emergency signalling, educational applications and basic communication systems.

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