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Traffic Light Controller Using FSM in Verilog HDL

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Abstract- Traffic Light Controller Using Finite State Machine (FSM) is a software-based VLSI project developed using Verilog Hardware Description Language (HDL). The main objective of this project is to design and simulate an automatic traffic light control system that operates in a predefined sequence. The system consists of three traffic signals: Red, Green, and Yellow, which represent STOP, GO, and CAUTION, respectively.A Finite State Machine (FSM) is used to control the transitions between these three states. The controller operates based on clock and reset signals, ensuring proper and systematic switching of traffic lights. Verilog HDL is used to describe the digital circuit, while a testbench is developed to verify its functionality through simulation. The project can be implemented and tested using software tools such as EDA Playground, ModelSim, or Icarus Verilog, along with GTKWave for waveform analysis.

Keywords— Traffic Light Controller, Finite State Machine (FSM), Verilog HDL, VLSI Design, Digital Logic Design, State Transition, Traffic Signal Control, Clock Signal, Reset Signal.

I. INTRODUCTION

A Traffic Light Controller Using Finite State Machine (FSM) in Verilog HDL is a digital system designed to control traffic signals automatically in a systematic and predefined sequence. Traffic light controllers play an important role in managing road traffic, reducing congestion, and improving safety at intersections. Traditional traffic signal systems use fixed timing mechanisms, while digital traffic controllers use programmable logic to provide accurate and reliable signal operations. This project focuses on designing and simulating an automatic traffic light controller using Verilog Hardware Description Language (HDL).

The main objective of this project is to develop a digital traffic light control system using a Finite State

Machine (FSM). An FSM is a sequential logic model that consists of a finite number of states and transitions between those states. In this project, the controller operates using three main states: Red, Green, and Yellow. Each state represents a specific traffic signal condition. The Red light indicates STOP, the Green light indicates GO, and the Yellow light indicates CAUTION. The controller switches between these states according to a predefined sequence based on clock signals.

Verilog HDL is used to describe the digital logic and behavior of the traffic light controller. It is widely used in Very Large Scale Integration (VLSI) design for developing and testing digital circuits. The controller is designed using sequential logic, where the state transitions are controlled by a clock signal. A reset signal is also included to initialize the system into its initial state and ensure proper operation. The FSM continuously changes its states in a fixed sequence, allowing the traffic signals to operate automatically without manual intervention.

The proposed system follows a simple operating sequence. Initially, the Red signal is activated to stop vehicles. After a predefined time interval, the controller changes to the Green state, allowing vehicles to move. Once the green signal duration is completed, the Yellow signal is activated to warn drivers that the signal is about to change. After the yellow signal duration, the controller returns to the Red state, and the sequence repeats continuously. This process ensures systematic switching of traffic lights and maintains proper traffic movement.

The project is implemented and verified using Verilog HDL simulation tools such as EDA Playground, ModelSim, and Icarus Verilog. A testbench is developed to provide clock and reset signals and verify the correct operation of the

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designed controller. Simulation waveforms can be observed using GTKWave to analyze state transitions and output signals. This helps identify design errors and confirms that the controller operates according to the expected sequence.

The Traffic Light Controller using FSM demonstrates the practical application of digital electronics, sequential circuits, and VLSI design concepts. It provides a simple and cost-effective approach to understanding automated traffic signal control systems. The proposed design can also be extended in the future by adding pedestrian crossing signals, vehicle sensors, emergency vehicle priority, and adaptive traffic control features to improve traffic management.

Overall, this project provides practical knowledge of Verilog programming, Finite State Machine design, digital circuit simulation, and functional verification.

II. WORKING

1. Initialization of the System
The Traffic Light Controller starts its operation when the power supply is provided to the digital system. A reset signal is used to initialize the controller and set it to its initial state. Initially, the FSM enters the Red state, where the Red light is turned ON, while the Green and Yellow lights remain OFF. This ensures that the controller starts from a known condition.

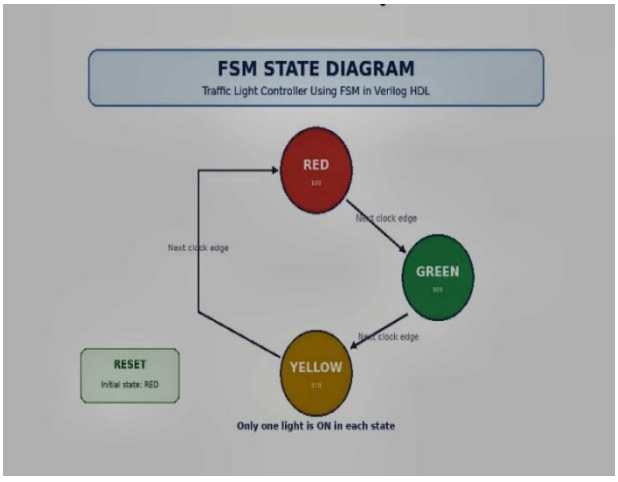
2. Red Light Operation
In the Red state, the Red traffic signal remains on for a predefined time interval. This signal indicates that vehicles must STOP and wait until the signal changes. The controller uses a clock signal and an internal counter to measure the duration of the Red light. After the specified time is completed, the FSM moves to the next state.

3. Green Light Operation
After the Red signal duration is completed, the FSM transitions to the Green state. In this state, the Green light turns ON, while the Red and Yellow lights remain OFF. The Green signal indicates that vehicles can MOVE safely. The controller maintains this state for a predefined time interval using the clock and counter mechanism. After completing the specified duration, the system moves to the Yellow state.

4. Yellow Light Operation
When the Green light duration is completed, the controller enters the Yellow state. The Yellow light turns ON, indicating CAUTION to drivers. It warns vehicles that the traffic signal is about to change from Green to Red. The Yellow signal remains active for a predefined time interval. After this interval, the FSM returns to the Red state.

5. State Transition and Repetition
The FSM controls the complete sequence of traffic signals using three states: Red, Green, and Yellow. The transitions between these states take place according to the predefined timing conditions. The sequence follows Red → Green → Yellow → Red. This process repeats continuously, ensuring automatic and systematic traffic signal operation without manual intervention.

6. Simulation and Verification
The complete traffic light controller is designed using Verilog Hardware Description Language (HDL). A testbench is developed to provide clock and reset signals and verify the functionality of the design. Simulation tools such as EDA Playground, ModelSim, and Icarus Verilog are used to execute and test the Verilog code. GTKWave is used to observe the output waveforms and analyze the state transitions. The simulation confirms that each traffic light operates in the correct sequence and for the specified duration.



Advantages

- Automatic Operation: Controls traffic lights automatically without manual intervention.
- Simple Design: Uses a simple FSM architecture with three states.
- Low Cost: Can be implemented using basic digital logic components.
- Reliable Performance: Provides systematic and predictable signal switching.
- Easy Implementation: Verilog HDL makes the design easy to develop and simulate.
- Fast Operation: Clock-based control ensures accurate state transitions.
- Easy Testing: Functionality can be verified using simulation tools.
- Low Power Consumption: Digital logic implementation requires relatively low power.
- Flexible Design: Signal timing can be modified according to requirements.
- Future Expansion: Additional features like pedestrian signals and emergency vehicle priority can be added.

Disadvantages

- Fixed Timing: Uses predefined timing for each traffic signal.
- No Traffic Detection: Cannot detect the actual number of vehicles.
- Traffic Congestion: Fixed timing may cause unnecessary waiting.
- Limited Functionality: Basic design supports only three traffic signals.
- No Emergency Priority: Does not automatically provide priority to emergency vehicles.
- Simulation Dependency: Requires simulation tools for design verification.
- Clock Dependency: Incorrect clock operation may affect signal transitions.
- Hardware Requirement: Practical implementation requires FPGA or other digital hardware.
- No Adaptive Control: Cannot adjust signal timing according to traffic density.
- Limited Real-World Application: Basic design requires additional features for practical traffic management.

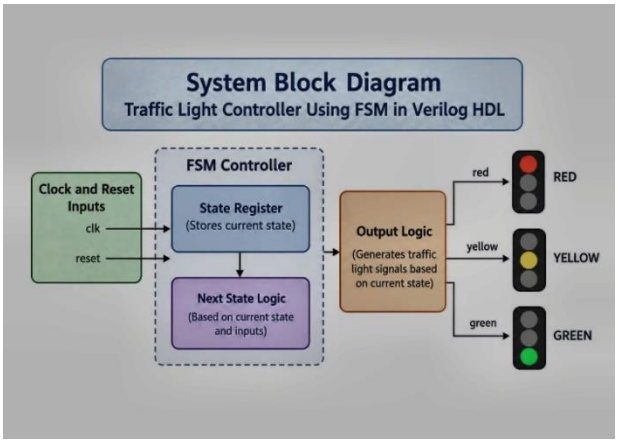


Figure 1: System Block Diagram of Traffic Light Controller Using FSM IN Verilog HDL

III. CONCLUSION

The Traffic Light Controller Using FSM in Verilog HDL successfully demonstrates the design of an automatic traffic signal control system using digital logic. The Finite State Machine controls the Red, Green, and Yellow lights in a predefined sequence using clock and reset signals. The design is simulated and verified using Verilog HDL and a testbench. The simulation results confirm the correct operation and state transitions of the controller. This project provides practical knowledge of FSM design, sequential circuits, and VLSI concepts. In the future, the system can be improved by adding vehicle detection sensors, pedestrian signals, and emergency vehicle priority to make traffic management more efficient and intelligent.

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