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Comparative Study and Design of High Performance Mixer

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Abstract

In recent time the use of RF mixer has been increased greatly. Gilbert cell is widely used as core of the mixer because it provides high conversion gain, good port-to-port isolation and low even-order distortion. It is found that the linearity of mixer is very good for Multi-Tanh technique by incorporating multiple differential trans-conductance stage but it reaches to very low conversion gain whereas, use of current bleeding technique increase linearity and conversion gain of the mixer by adding current source to increase the bias current at the expense of power consumption. Since, CMOS technology has become dominant because of its several advantages such as low cost, low static power dissipation and low area, the design of low noise amplifier using CMOS technology was top choice for design of Low Noise Amplifier. The single ended and differential LNA was designed to operate in a WCDMA reception range using a BSIM3V2 model (Level 49) CMOS UMC 0.18µm technology in Xcircuit Open source EDA tool. The key issues in the design, gain, noise and linearity were considered. The LNA's was designed to provide high gain, matching to 50Ω RF system, good linearity.

Keywords- Ultra-wideband (UWB), Differential mode of application, cross coupled feedback, Direct – Coupled amplifier.

I. INTRODUCTION

Wireless communication market demands mainly in the last decade. The requirement of high frequency Trans receivers has been unstable& unexpected. Wireless products demand low cost, low power, high speed and high volume. Due to the improvement of integrated circuit (IC) Technology, the size of electronic components like transistors has consistently reduced. In addition reduction in channel length to improvement in unity gain, cut of frequency (ft) and maximum operating frequency (Fmax), which shows the potential of CMOS at the front end of the RF system [1].The reduction in supply voltages makes the design of analog RF circuits more challenging. On the other hand the RF circuits are usually designed by passive components, like resistors, capacitors & inductors and size of these components does not scale proportionally. As a result, the chip area does not reduce to the same extent. Hence there is a need to build a complete trans-receiver on a single CMOS chip to minimize the silicon area as well as cost.

Efforts has been made to design digital processing functions, as close to the front end as possible but still most of the RF front end components like low noise amplifier and mixer are still designed in analog domains. Due to advancement of component level the channel lengths as well as width continue reduces. The transistor occupies less silicon area and switch fast e.g. the super hetero dyne architecture [2] is the most popular architecture in modern RF receivers. The second component of wireless receiver front end is a low noise amplifier (LNA). Its main function is to amplify the signal with low noise for substituent stages [3].

Third component of receiver front end is a mixer. Mixer translates an incoming RF signal to a lower frequency called intermediate frequency (IF).The output consists of multiple images of the input signal where each image is shifted up or down by multiplies of LO frequency. Mixer is generally classified as active and passive. Conversion gain is the main difference between both classes. Active mixer can achieve high conversion gain and require low local oscillator (LO) power then passive counter parts.

Active mixer reduces noise contributed to the subsequent stages of the receiver which are widely used in RF applications. Passive mixer, on the other hand, typically show conversion loss but exhibit excellent intermediation (IM) performance, high linearity and speed with high LO power requirements and find their applications in microwave & base station circuit [3].Various types of active mixer have been presented for receiver front end. In this thesis the resistive load Gilbert cell mixer topology has been design. They provided good linearity & high gain performance.

II. REVIEW OF TECHNIQUES

The frequency band of 2.4GHz is widely being used in communication systems. This band used in WLAN802.11b standard and Bluetooth. This standard is mostly used in modern communication system. There is a great need for trans-receivers which is capable of working with this frequency standard [4]. From an RF front end point of view, the receiver architecture is not much of difference.

The LNA and mixer required in all receiver topologies. The mixer design discuss in this thesis are applicable for most of the receiver design. The mixer is the intermediate sub system after the LNA unless the load of LNA is external filter in which the performance of LNA needs to be measured individually and the output of LNA needs to match to certain inputs. CMOS circuits have excellent switching property that is an important requirement for digital circuit design.

Therefore, CMOS technology has been dominated for digital circuits in VLSI industry. Due to this perfect switching property. The high performance mixer that is based on switch has been realized by MOS transistor called as MOS passive switching mixers [7]. There are four transistors in MOS passive switching mixer these transistors are driven by anti-phase signal. Therefore, only two transistors which are driven by the same phase signal are ON at any given point of time. The perfect switching property hold for the assumption of a sufficiently large input LO+(OR LO-) being used to fully turn ON or OFF the transistors.

For an ideal square wave input signal, the voltage gain of a mixer is equal to MOS phase shift switching mixer has an excellent linearity performance [7].It does not require bias current. This property has great advantage for homodyne trans-receiver. However, there are some drawbacks in this type of mixer. It requires a large voltage drive to achieve fully ON/OFF switching of the transistor. The coupling through the gate to source capacitor cause high LO – RF and RF-IF feed through.

In[8], a source follower based mixer design has been presented which is suitable for low power receiver. This mixer shows an outstanding linearity performance by using the unbalanced source coupled pair operation. However, the LO-IF feed through is high with no gain. The overall performance is not much better than the passive switching mixer.

The majority of popular CMOS mixer topologies are based on the traditional bipolar double balanced cross coupled differential modulator stage introduce by Gilbert [9].The core part of Gilbert cell mixer resembles the Gilbert analog multiplier. The transistor has designed to operate in the active region. This type of mixer operates on a switched current principle. The output of the circuit depends on the Trans conductance of the cross couple pair and the bias current. The advantage of Gilbert cell multiplier is high gain low port to port feed through [4]. However, this type of multiplier requiresat least three transistors. This structure has a drawback for low voltage operation of the mixer.

The mixing operation can also be performed by using the body terminal of a MOS transistor [10]. This type of mixer is called Body Injection Mixer. In this topology, the number of stacked transistors can be reduced so that the supply voltage can also be reduced. However, the conversion gain is low and the noise performance deteriorates as the input to body terminal makes the substrate noisier.

III. PROPOSED METHODOLOGY

The RF signal from the antenna which is amplified by the low noise amplifier of high frequency. These signals need to be converted to digital for digital signal processing. In order to ensure signals can undergo proper signal processing they are down converted to lower intermediate frequencies (IF) and then passed forward. Gilbert mixer is used in this work to gives differential output signal.

An active double-balanced CMOS Gilbert cell mixer was designed and fabricated in a UMC 180nm CMOS process. An all NMOS Gilbert cell topology was used in design to achieve high frequency operation. The double balanced mixer has differential inputs. The mixer takes differential inputs at RF and also LO ports so that a better noise performance can be achieved. The NMOS transistor of the mixer core are biased near to their threshold voltage across the transistors is also reduced using near threshold biasing to further reduced voltage supply requirement. Table 3.1 gives the component values. For Gilbert cellMixer RF models of transistor has been used.

Table I Component value for Mixer Design.

Component	Value
Lall transistor	0.18µm
WM2,M3,M8,M11	25µm
WM4,M8,M12	105µm
R6,R7,R8	650,650,750Ω

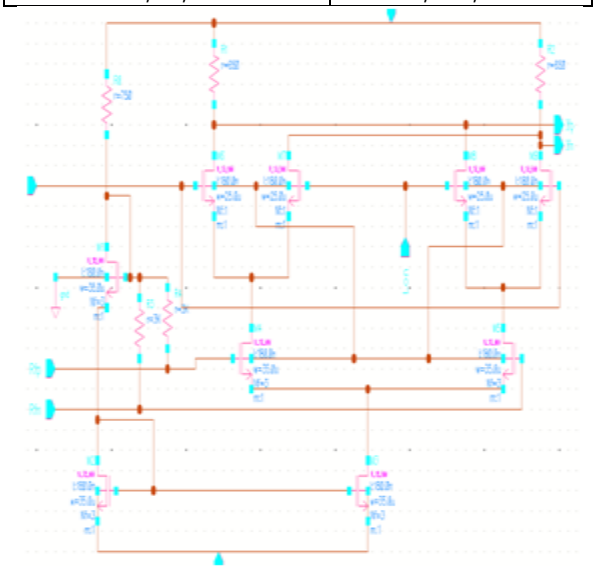

Figure 1 Schematic of Proposed Mixer with Biasing Circuitry.

The mixer circuit with biasing circuitry is shown in figure 3.1 the bias current for the mixer core and the output buffer stage is regulated by current mirror through transistor M7-M8. Transistor M6-M7 perform a V-I conversion on differential RF signals that will be mixed with the differential LO signals. Transistor M1, M2, M3, M4 operates as switches to perform the frequency translation.

The 650Ω Resistive load is chosen for high frequency operation.

Figure 1 shows the test bench for proposed mixer. In which the symbol of the Gilbert cell mixer is connected to additional required circuitry to analyses the mixer. Here we supply the input LO voltage of 2.25GHz frequency directly to the LO port of the Mixer through a voltage source (port2).RF port of the mixer is connected to the balun which supply the differential input RF signal through a single source (port1).Output IF signal is measured through port3. The mixer is operated at 1.8V power supply.

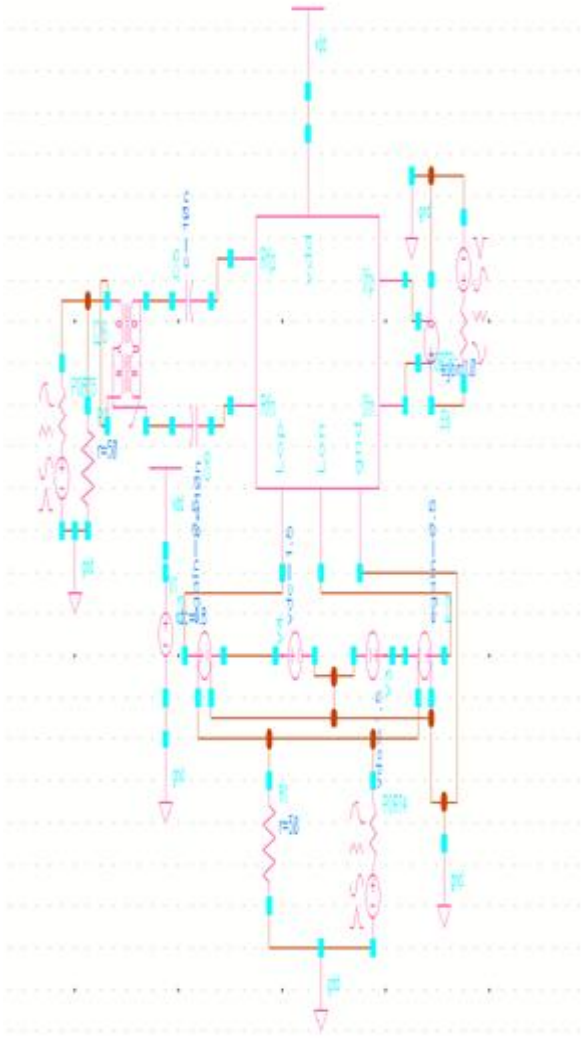

Figure 2 Test Bench for Proposed Mixer.

1. Proposed Flow Chart

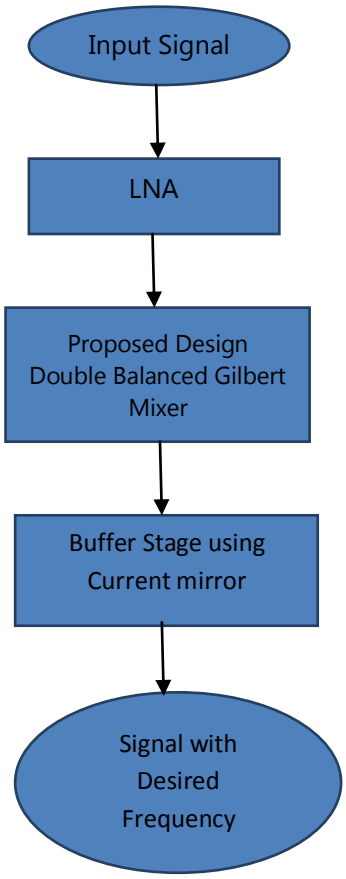

Figure 3 Proposed FlowChart.

Proposed mixer topology employ LNA at first stage for amplifying the signal and without adding too much noise then we added a mixer which will produce a frequency of desire range having a good gain and better noise performance. at last buffer circuit or current mirror is used for maintaining contant current.

Algorithm:

1. Get input from user with low amplitude and certain frequency
2. Implementation of LNA for amplifying the signal.
3. Formation of Gilbert cell mixer block The Gilbert cell mixer or Gilbert cell multiplier is a form of double balanced mixer that is able to exploit the symmetrical topology to remove the unwanted RF & LO output signals from the IF by cancellation
4. Formation of Cascode amplifier for providing large gain.
5. Implementation of current mirror for obtaining constant current.

IV. SIMULATION RESULT OF MIXER

The mixer circuit is simulated in magic simulator. The mixer is designed to operate at 1.8V voltage. Figure 4.1 to 4.8 shows the simulation results of the proposed mixer. Measured voltage conversion gain (Swept PSS with PAC) is around 6.7dB shown in the figure 4.1. The noise figure of mixer has been found to 15.5dB (figure 4.2) input and output impedance of the mixer are set to 50Ω.

The linearity performance is measured using two-tone-test.A second input signal is input to the RF ports of the mixer. The RF signal frequency is at 2.4GHz, and the second input signal frequency is at 2.401GHz. Figure4.1 and 4.2 shows the simulation result of the boy fundamental output power and the third order intermediation distortion power as a function of input power. Figure 4.3 shows the plot of the Input-referred IP3 measured to 1.5dBm and the 1-db compression point is found to -11 dBm shown in figure 4.4. The power consumption of the mixer is around 10.0 mW for 1.8V power supply.

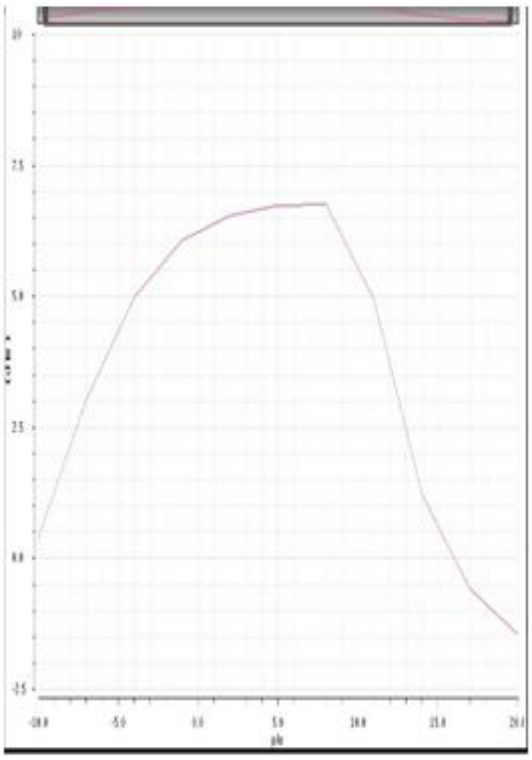

Figure 4 Conversion Gain of Proposed Mixer (Swept PSS with PAC).

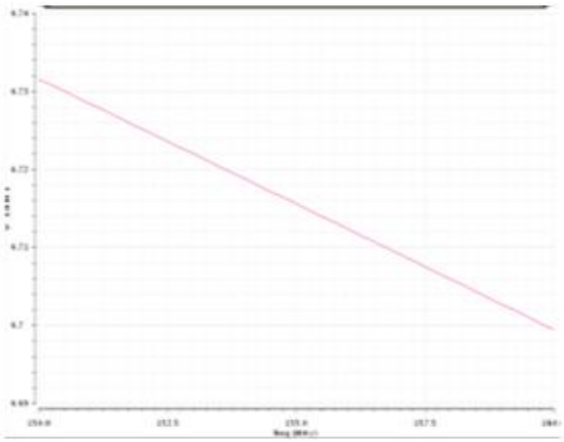

Figure 5: Conversion Gain of Proposed Mixer (PSS with Swept PAC).

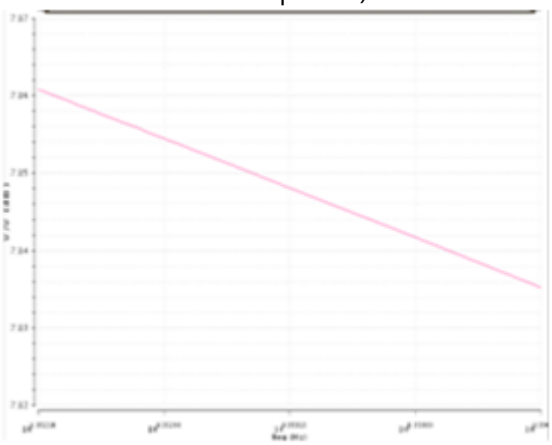

Figure 6: Conversion Gain of Proposed Mixer (PSS with Swept PXF).

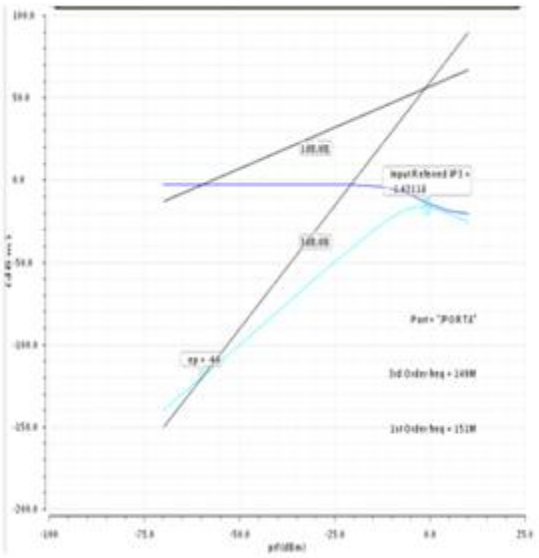

Figure 7: Third Order Intercept point.

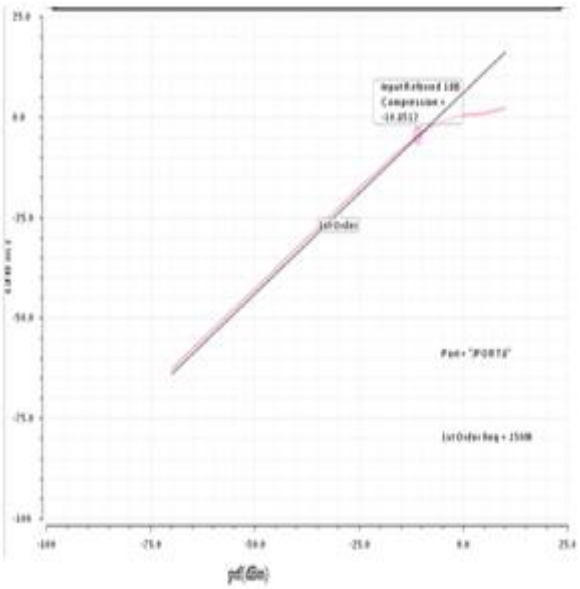

Figure 8: 1dB Compression Point.

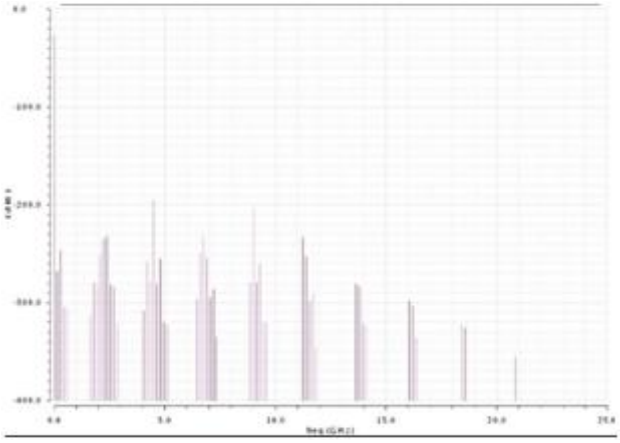

Figure 9: Power Consumption of a Proposed Mixer.

1. Two Input Transconductance Stage Of The Proposed Mixer

Barrie Gilbert present multitanh principle with bipolar transistors. So this thesis uses the multi-tanh technique to design some new Structure in order to improve linearity and gain. First we double. The Trans conductor level with four NMOStransistors the design implemented in UMC 0.18um CMOS process and operated at 2.4GHz with 1.8V power supply. Components and their value are listed below:

Table 2 Components value for Two input Trans Conductance stage Mixer.

Component	Value
LAll Transistor	0.18 µm
WM-M1,M2,M3,M4	80µm
WM-M5,M6,M7,M8,M9,M10,M11,M12	120µm
LoadResistor-R1,R2,R3	500Ω

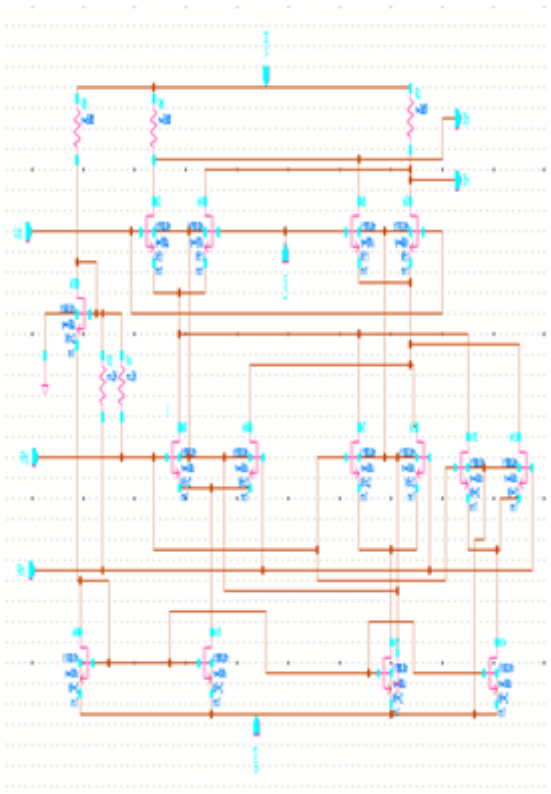

Figure 10: Schematic of Double Trans conductance stage Mixer.

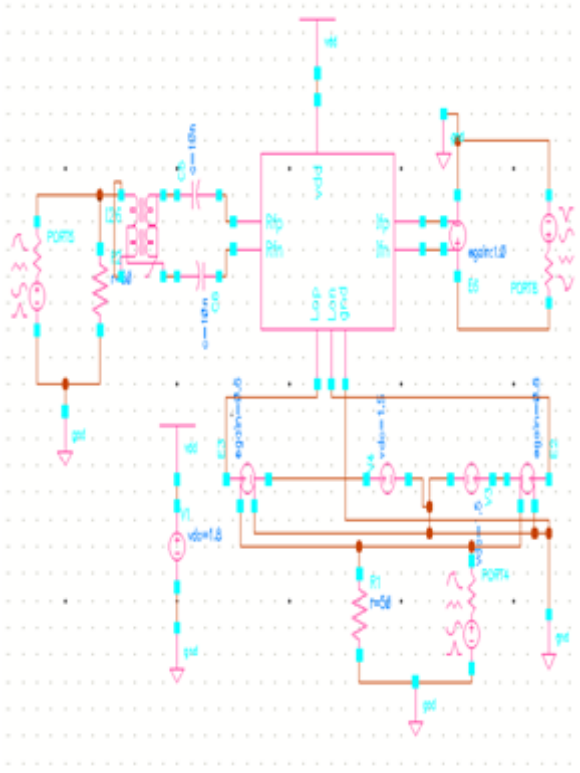

Figure 11: Test Bench of Double Trans conductance stage Mixer.

The mixer circuit with biasing circuitry is shown in figure 4.15 the bias current for the mixer core and the output buffer stage is regulated by current mirror through transistor M11 to M14. Transistor M5 to M10 perform a V-I conversion on differential RF signals that will be mixed with the differential LO signals. Transistors M1, M2, M3, and M4 operate as switches to perform the frequency translation. The 500Ω Resistive load is chosen for high frequency operation.

Figure 4.16 shows the test bench for proposed mixerin which the symbol of the Gilbert cell mixer is connected to additional circuit to analyses of mixer. Here we supply the input LO voltage of 2.25GHz frequency directly to the LO port of the Mixer through a voltage source (port2).RF port of the mixer is connected to the balun which supply the differential input RF signal through a single source (port1).Output IF signal is measured through port3. The mixer is operated at 1.8V power supply.

2. Simulated Result of Mixer

The mixer circuit is simulated in magic using simulator. The mixer is designed to operate at 1.8V voltage. Figure 4.15 to 4.18 shows the simulation results of the proposed mixer. Measured voltage conversion gain (Swept PSS with PAC) is around 12.5dB shown in the figure 4.15. The noise figure of mixer has been found to 15.5dB in figure 4.18. The input and output impedance of the mixers are set to 50Ω.

The linearity performance is measured using two-tone-test.A second input signal is input to the RF ports of the mixer. The RF signal frequency is at 2.4 GHz and the second input signal frequency is at 2.401GHz. Figure 4.16 shows the plot of the Input-referred IP3 measured to -1dBm and the 1-db compression point is found to -10dBm shown in figure 5.11. The power consumption of the mixer is around 10.0 mW at 1.8V power supply.

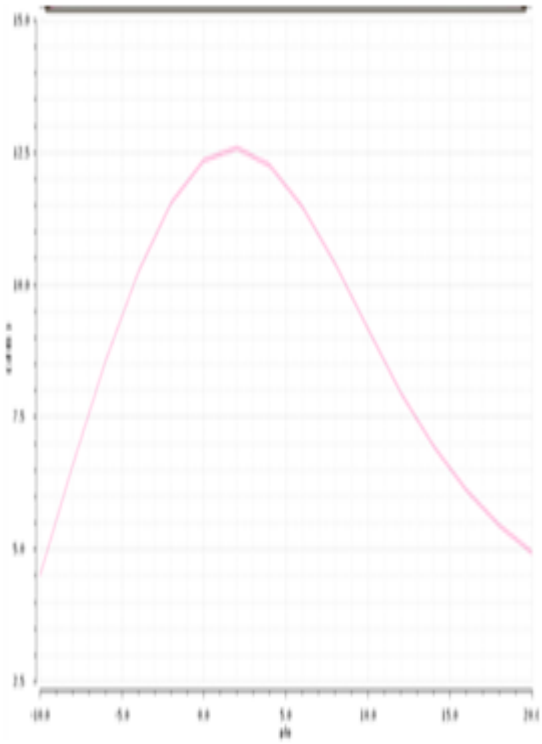

Figure 12: Voltage Conversion Gain (swept PSS with PAC).

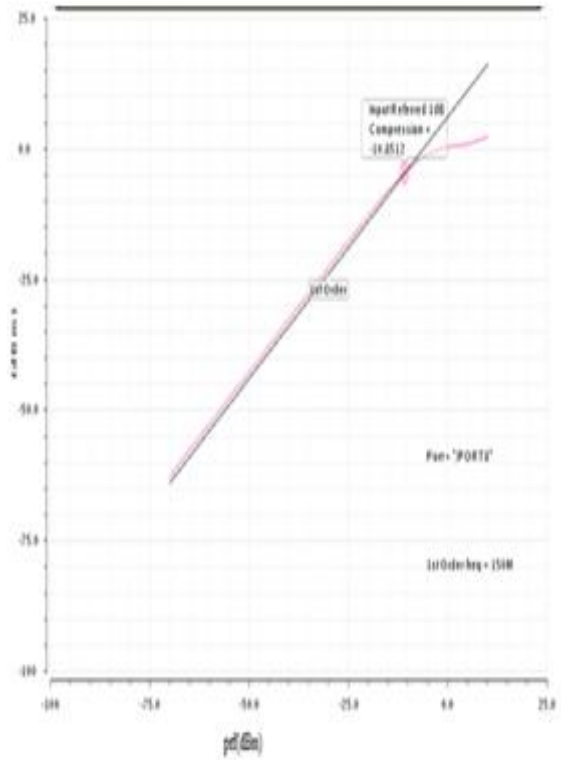

Figure 13: 1dB Compression point.

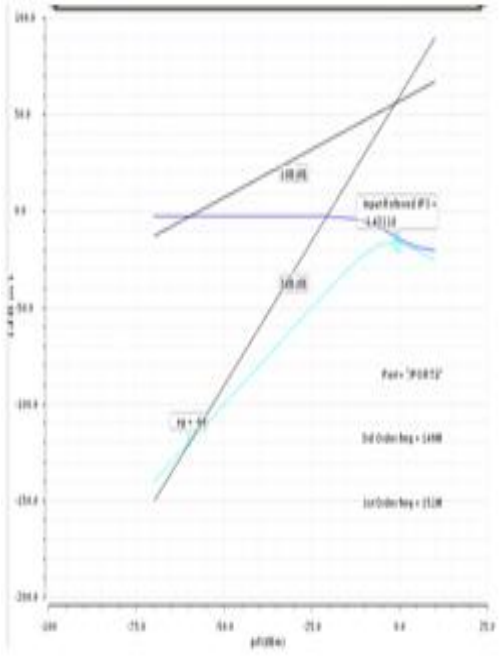

Figure 14: Third order Intercept Point.

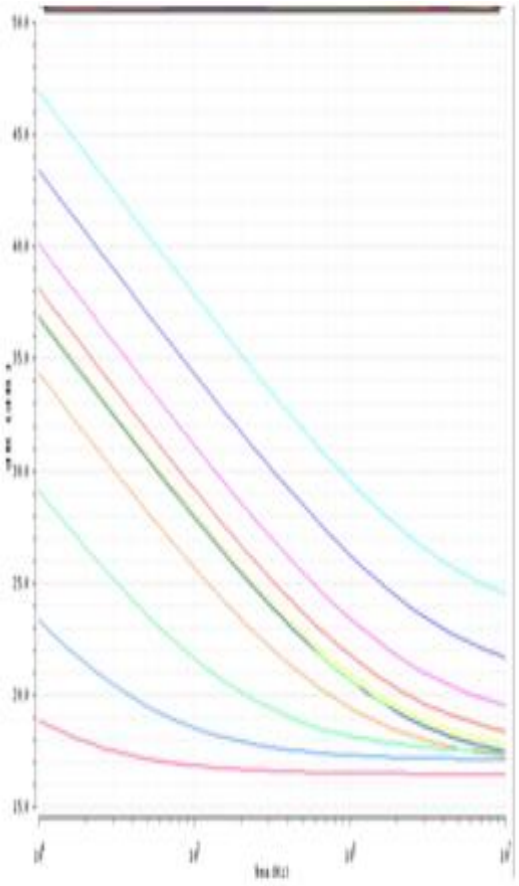

Figure 15: Noise Figure of Proposed Mixer.

3. Three input Trans conductancestage of the Proposed Mixer

Barrie Gilbert presented a multi-tanh principle with bipolar transistors. So this thesis uses the multi-tanh

technique to design some new Structure in order to improve linearity and gain. Secondly we triple the transconductance level with six NMOS transistors the design implemented in UMC 0.18 µm CMOS process and operated at 2.4 GHz with 1.8V power supply. Components and their value are listed below:

Table 3 Component value for Three input transconductance Stage Mixer.

Component	Value
LAll Transistor	0.18 µm
WM-M1,M2,M3,M4	80µm
WM-M5,M6,M7,M8,M9,M10,M11,M12	120µm
LoadResistor-R1,R2,R3	500Ω

The mixer circuit with biasing circuitry is shown in figure 4.7 the bias current for the mixer core and the output buffer stage is regulated by current mirror through transistor M10-M11-M12. Transistor M6-M7-M8-M9 perform a V-I conversion by differential RF signals that will be mixed with the differential LO signals. Transistors M1, M2, M3, and M4 operate as switches to perform the frequency translation. The 500Ω Resistive load is chosen for high frequency operation.

Figure 4.8 shows the test bench for proposed mixer. In which the symbol of the Gilbert cell mixer is connected to additional circuit to analyze of mixer. Here we supply the input LO voltage of 2.25GHz frequency directly to the LO port of the Mixer through a voltage source (port2).

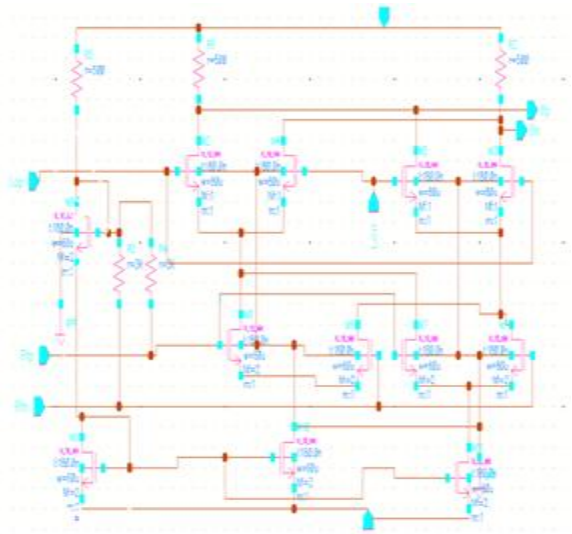

Figure 16: 16.Schematic of Double Trans conductance stage Mixer.

RF port of the mixer is connected to the balun which supply the differential input RF signal through a single source (port1).Output IF signal is measured through port3. The mixer is operated at 1.8V power supply.

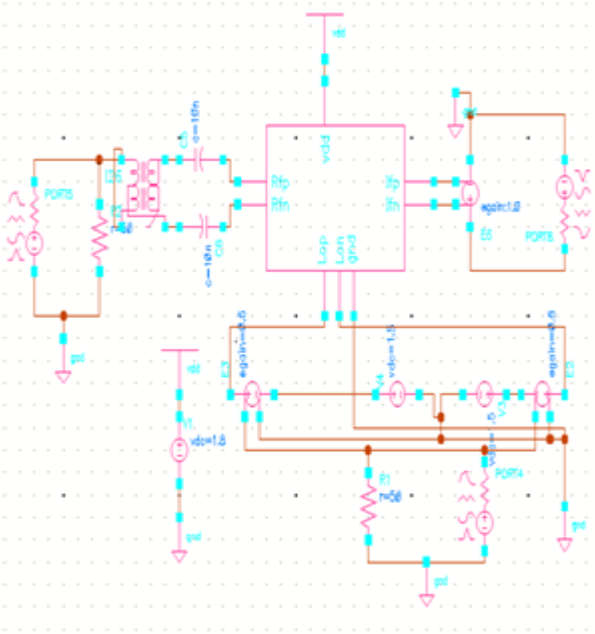

Figure 17: Test Bench of Double Trans conductance stage Mixer.

4. Simulated Result of Mixer

The mixer circuit is simulated in magic using simulator. The mixer is designed to operate at 1.8V voltage. Figure 4.15 to 4.18 shows the simulation results of the proposed mixer. Measured voltage conversion gain (Swept PSS with PAC) is around 12.5dB shown in the figure 4.15. The noise figure of mixer has been found to 15.5dB in figure 4.18. The input and output impedance of the mixers are set to 50Ω.

The linearity performance is measured using two-tone-test.A second input signal is input to the RF ports of the mixer. The RF signal frequency is at 2.4 GHz and the second input signal frequency is at 2.401GHz. Figure 4.16 shows the plot of the Input-referred IP3 measured to -1dBm and the 1-db compression point is found to -10dBm shown in figure 5.11. The power consumption of the mixer is around 10.0 mW at 1.8V power supply.

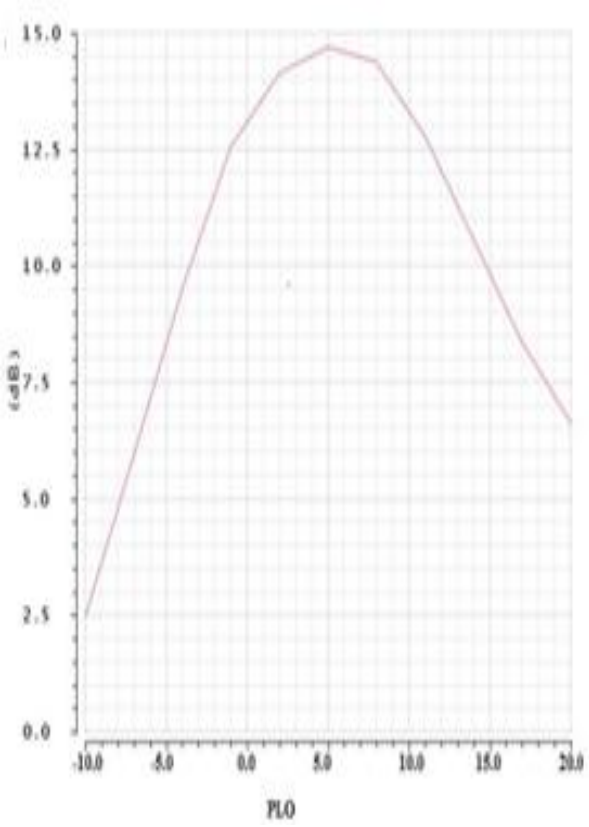

Figure 18: Voltage Conversion Gain(Swept PSS with PAC).

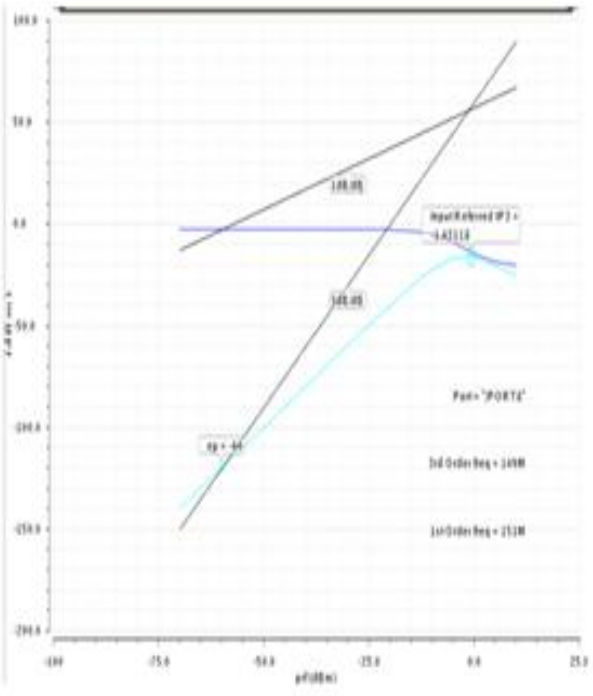

Figure 19: Third Order Intercept Point.

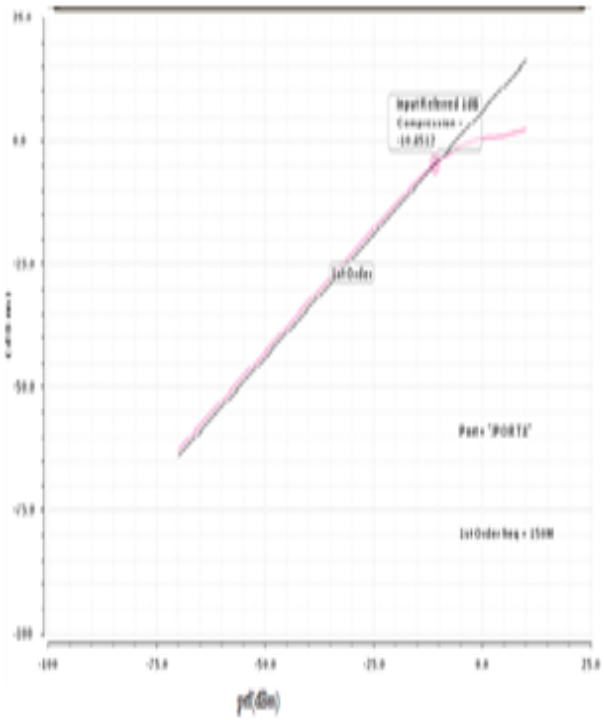

Figure 20: 1dB Compression Point.

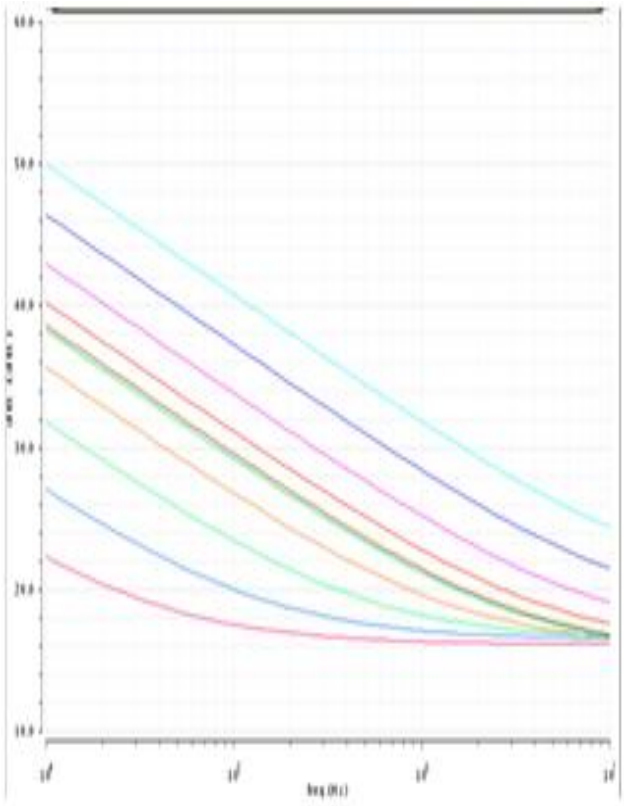

Figure 21: Noise Figure.

5. Layout Design Of Mixer

This section presents the Layout view of the proposed Gilbert Mixer. The layout has been carried out in 180nm CMOS technology in virtuoso editor of

the magic. The layout of RF integrated circuited circuits plays an important role in proper circuit functioning of a chip. The parasitic of wires for routing of signals degrade the performance of ICs and need to be minimized by design proper layout. Following points were considering while doing the layout of the Mixer.RF modal of transistor were used instead of conventional transistors. Thick metal layer Metal-6 has been used for routing of input and output signals due to its low resistivity and maximum distance from the substrate which results in low parasitic capacitance. Figure 4.19 shows the layout design of the resistive load Gilbert cell mixer. The layout has been checked successfully.

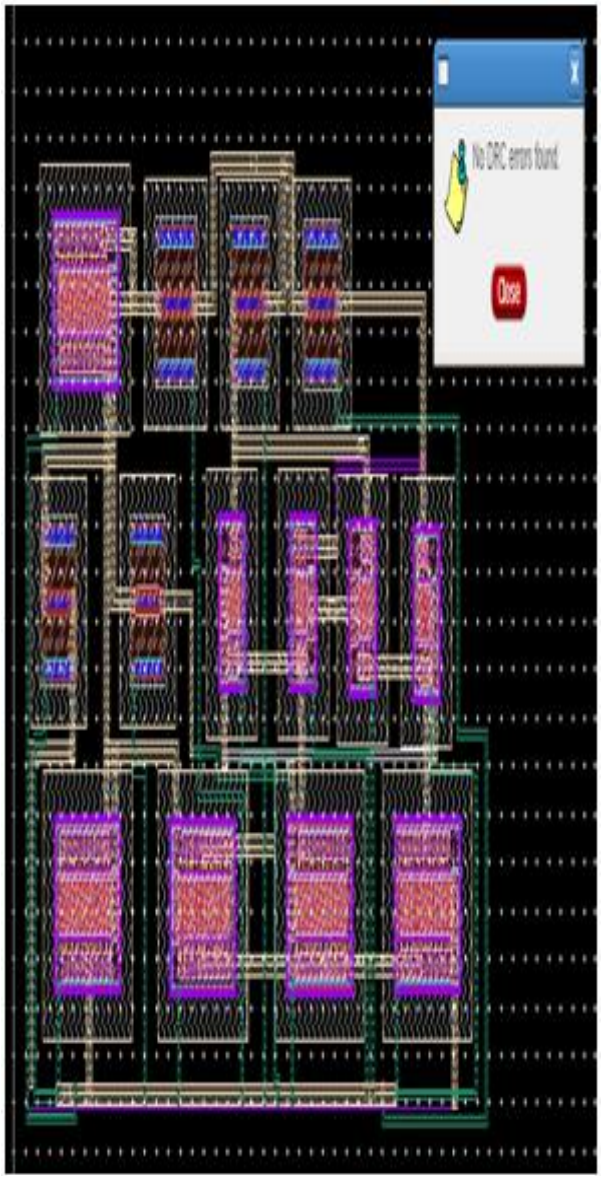

Figure 22: Layout view of the Gilbert Mixer.

V. COMPARISON OF THE OLD AND NEW WORK

Table 4 Comparison of The Existing Work And Proposed Work**.**

S.No.	Parameter	Existing Work	Proposed Work
1	Input RF Frequency	12.5	12.4GHz
2	Input LO Frequency	12.5	2.25GHz
3	Supply Voltage	1.5	1.8V
4	Technology	0.13	180nm
5	Conversion Gain	3db	6.7dB
6	Noise Figure	15.5dB	15.2dB
7	1-Db Compression Point	1.62dBm	-10dBm
8	IIP3	-16.6dBm	-1dBm
9	Power Consumption	45mW	10mW

Table -5: Measured result of the two input Tran conductance Stage Mixer.

S.No	Parameter	Proposed Work
1	Input RF Frequency	12.4 GHz
2	Input LO Frequency	12.25 GHz
3	Supply Voltage	1.8V
4	Technology	180nm
5	Conversion Gain	12.5dB
6	Noise Figure	15.2dB
7	1-Db Compression Point	-10dBm
8	IIP3	-1dBm
9	Power Consumption	20mW

Table -6: Measured result of three input Trans conductance Stage Mixer.

S.No	Parameter	Proposed Work
1	Input RF Frequency	2.4GHz
2	Input LO Frequency	2.25GHz
3	Supply Voltage	1.8V
4	Technology	180nm
5	Conversion Gain	7.5dB
6	Noise Figure	15.2dB
7	1-Db Compression Point	-10dBm
8	IIP3	-1dBm
9	Power Compression	30mW

VI. CONCLUSION

Represents the design and implementation of the Gilbert mixer. It represents the proposed mixer for down conversion of input RF signal to IF signals. Double balanced cell mixer topology has been used in this thesis due to the improved feed through performance and achieved good linearity. Circuit design and simulation result of the mixer are presented in chapter 5. In this a mixer 2.4 GHz input signal is mixed with 2.25GHz local oscillator signals and produced an output IF signals of 150 MHz simulation results presented in chapter 5 represented the characteristic for the conversion gain, noise figure and linearity performance. All parameters are appropriate and meet the desired specification Table 5.1 gives the values for simulated parameters of proposed mixers.

Future Work

Mixer presented in this thesis is appropriate for the RF receiver front-end application. Furthermore input pairs can achieve higher linearity, but power consumption will increase at the same time.

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