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High Performance Low Noise Amplifier for RF Application

M.Tech. Scholar Shradha Chouhan Asst. Prof. Priyanshu Pandey
Dept. of Elctronics & Communication & Engg.
Patel College of Science and Technology,
Chouhan1993@gmail.com
Indore, MP, India

Abstract

Recently, In RF application the use of Low noise amplifier is highly versatile and majorly used in modern wireless communication like Wi-Max, WLAN, GSM, Bluetooth and satellite communication. Low Noise amplifier have important feature like signal amplification with rejection of noise. Low noise amplifier in modern communication used as filter with amplifier. In recent scenario low noise amplifier available in wide band, single band, multi-band frequency of application. Along with that the Low noise amplifier must be capable of reduces the reflection of signal exist by elements and connecting interface inside the amplifier. Low noise amplifier available with high gain, noise rejection and with less power consumption. In this paper review the work of past decades done in low noise amplifier. Low Noise Amplifier (LNA) is versatile used in every communication system, low noise amplifier, power amplifier and Darlington amplifier. Today technology required high speed of transmission efficiency with small power consumption and less utilization of elements in proposed amplifier, Low Noise Amplifier (LNA) products full fill all requirement of modern wireless communications, so that review and discussion, future requirement of technology is needed to discuss. In this paper discusses issues of low noise amplifier, its application, issues and recent trends. This paper review some techniques of Design of Low Noise Amplifier (LNA) to improve performance of communication system.This work has been carried out in Gspice open source simulator and the layout has been designed in Magic EDA Layout designing tool.

Keywords- Multi-Tanh, Current Bleeding Technique, Switched Biasing, Folded Cascode, Bulk-Driven, CCPD, MGTR.

I. INTRODUCTION

RF industry has changed quite a bit since the days of Marconi and Tesla-both the men who enabled radio communications. Modern radio frequency engineering is an exciting and dynamic field, due to the beneficial interdependency between recent developments in electronic device technology and the increase in demand for voice, data, and video communication capacity [1]. Prior to this revolution in communications, RF technology was the nearly exclusive domain of the defense industry but the recent increase in demand for communications systems with applications such as wireless paging, Broadcast video, Bluetooth transceiver, Wi–Fi (WLAN), Wi-Max, CDMA, WCDMA, EGPRS, GSM and many more is revolutionizing the industry. RF technology is important for these applications because these require high operational frequencies which allow both large numbers of independent channels as well as significant available bandwidth per channel for high speed communication [2-3]. Figure 1.1 shows some disciplines that requires RF design. The field of design in the electronics system that employs RF and Microwave Engineering includes the frequencies ranging from 300 kHz to over 100 GHz.

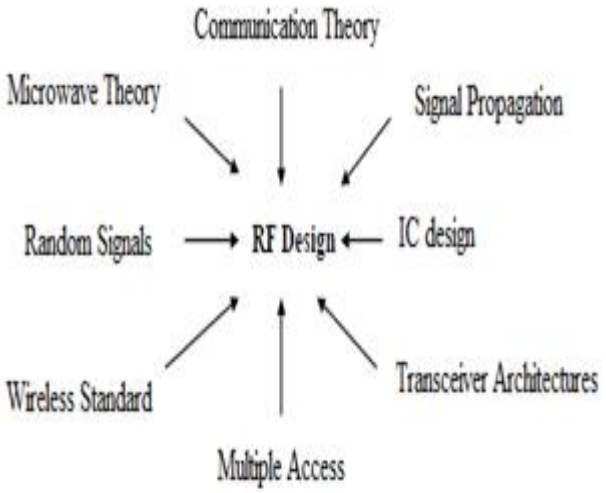


Figure 1: showing disciplines require RF Design.

RF engineering refers to the circuits/devices operating in the frequency range 300 kHz to over 1 GHz while the microwave engineering refers to the circuits/devices operating in the frequency range between 300 kHz or 1 GHz to over 100 GHz.

II. LITERATURE SURVEY

Present two monolithic microwave integrated circuit (MMIC) cryogenic broadband low-noise amplifiers (LNAs) based on the 100 nm gate length InP high-electron mobility transistor technology for the frequency range of 0.3–14 and 16–28 GHz. The 0.3–14 GHz three-stage LNA exhibited a gain of 41.6 ± 1.4 dB and an average noise temperature of 3.5 K with a minimum noise temperature of 2.2 K at 6 GHz when cooled down to 4 K. The 16–28 GHz three-stage LNA showed a gain of 32.3±1.8 dB and an average noise temperature of 6.3 K with a minimum noise temperature of 4.8 K at 20.8 GHz at the ambient temperature of 4 K. This is the first demonstration of cryogenic MMIC LNA covering the whole K-band. To the best of the authors' knowledge, the cryogenic MMIC LNAs demonstrated the state-of-the-art noise performance in the 0.3–14 and 16–28 GHz frequency range [11].

he linearity and noise requirements in multi-band multi-standard applications make the design of RF CMOS circuits very challenging. A wideband low-noise transconductance amplifier (LNTA) in CMOS 0.13 mm technology that operates between 1-6 GHz is presented. The LNTA is based on a shuntfeedback (SFB) amplifier with current-reuse scheme and employing the noise-canceling technique used in low-noise amplifier designs for wideband input matching. Simulation results show a good trade-off between noise and power-consumption across the frequency span with an average noise figure of 4 dB and a minimum transconductance of 42 mS over the entire band. Performance variations were estimated at 2 GHz with Monte Carlo analysis. The total power consumption is 8.4 mW from 1.2 V supply [12].

Emerging new wideband standards likes UWB imposes new demands for wide band front-end systems. First of all, understanding of the specifications is needed to determine system requirements. Secondly, to design a front-end with a fractional bandwidth requires a good knowledge about underlying theories and techniques. The specifications of UWB are mentioned in [13]. Since UWB provides large bandwidth, high data rate, low power dissipation and low noise, so UWB is a better option for designing a low noise amplifier for RF Receivers.

There are various topologies to design an UWB LNA i.e. common gate, common source with cascade configuration and inductively degenerated common source topology. a design of low power differential LNA (low noise amplifier) in 130nm CMOS technology for 2.45GHz ISM band application is reported in this paper. The circuit involves several gm (tans- conductance) Enhancement techniques. These techniques provide high gain and reduce noise figure in spite of low intrinsic gm of the MOS transistor. And also the circuit is fully inductor- less. A prototype has been implemented producing a gain of 20dB with 4dB noise figure while dissipating power 1.45mw [14].

In another design a CMOS-RF digitally programmable gain amplifier gain is implemented as a part of a low power RF tuner IC using 180nm CMOS technology. "an improved of 13dB IIP3 is achieved without degrading with other parameter such as gain, NF, CMRR ". New concept of differential circuit trans- conductance is introduced which employs "Second order derivative of gm cancellation technique" and is called as differential multiple gated transistor [15]. [16] Proposed CMOS RFPGA LNA in D-TV application as a part of low power RF-tuner IC. This receiver employs a positive type image rejection

mixer for linearity and noise performance, 1/f noise get reduced with high linearity is achieved.

[17] Reports a simple three stage amplifier which works for UWB application, it uses simple current reuse topology with resistive feedback. The design will provide high gain of 15.5dB with very low noise figure.

Another work Describe an LNA based on "series shunt topology", this broadband LNA is able to provide gain of 10db and NF of 3.5 db. A two loop amplifier is consider whose input and output impedance obtain by providing same gain [18].

[19] Employs a common gate low noise amplifier using current reuse technique proposed for both UWB and low power consumption. The CG amplifier employed at the input stage; enable wideband input matching at low trans- conductance and frequency independent noise figure compare to common source amplifier. This technique (CG) is used in order to reduce the power dissipation with achieving reasonable power gain. The proposed LNA obtain 3dB bandwidth from 2.4 to 11.2GHz minimum NF of 3.9dB, it consumes power of 3.4mw at 1.8v and complete process is carried out in 180nm technology.

III. PROPOSED CIRCUIT DIFFERENTIAL LNA AND FLOWCHART

If the trans-conductance is increases then the overall gain will also get increases from equation 4.1 the value of trans-conductance will depend on W/L ratio of transistor.
Its mathematical expression is given as

$$g_m = \mu_n C_{ox} \frac{W}{L}(v_{gs} - v_{th}) \qquad (4.1)$$

As per requirement author have decrease the width of transistor to improve the linearity of LNA. And for maintaining noise figure authors have connected differentially.
Since in differential configuration only even order nonlinearities cancels while the odd order nonlinearities of the two transistors gets added and most of designers are concerned with the odd-order nonlinearities that generates IM3 distortion, there is no benefit of using the differential LNA's over their single-ended counterparts also we will have to bias the differential pair at the same to get the same IM3 distortion as that of a common-source stage. The reasons for going to differential circuits are many and most relate to IC implementations. Typical IC mixers have differential inputs, so we must do that conversion somewhere. NF may be worse but compared to what? Looking at the losses in front of the LNA (filters, duplexers, switches, components, etc.) and we find the LNA is not the biggest contributor. The most compelling reason though is elimination of common mode effects. The differential LNA gain is not impacted by large common-mode impedances to ground. Ideally there is no RF feedback across common-ground ties. This enhances stability. Not all antennas are single-ended.

Another reason for using differential stages in receivers is that bond wire and pins have values in the order of a few nH. In differential circuits the current flowing through the LNA remains constant. This implies less drop across the bond-wire over the differential case. In the single ended LNA would not have a constant current consumption with respect to time thus generate an AC induced voltage drop across the bond-wire on the ground and VCC pins. Common mode and substrate noise injection effects are vastly reduced in differential pairs over single ended types. Single-ended circuits have no immunity to these effects, mixed signal chips are especially prone to this effect due to digital and baseband functions combine with RF circuits.

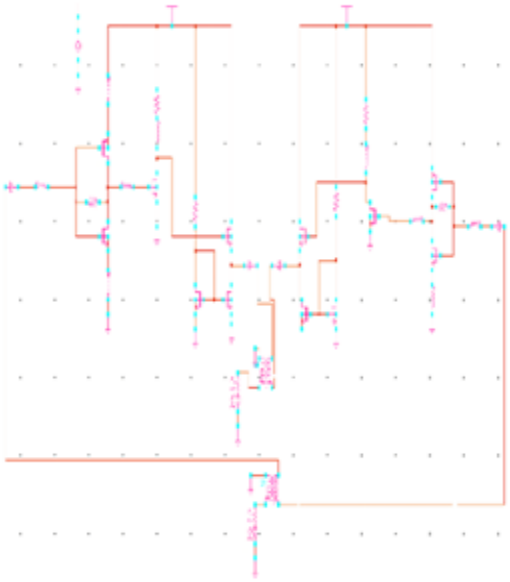


Figure 2: Proposed differential LNA.

1.Flowchart of Proposed System

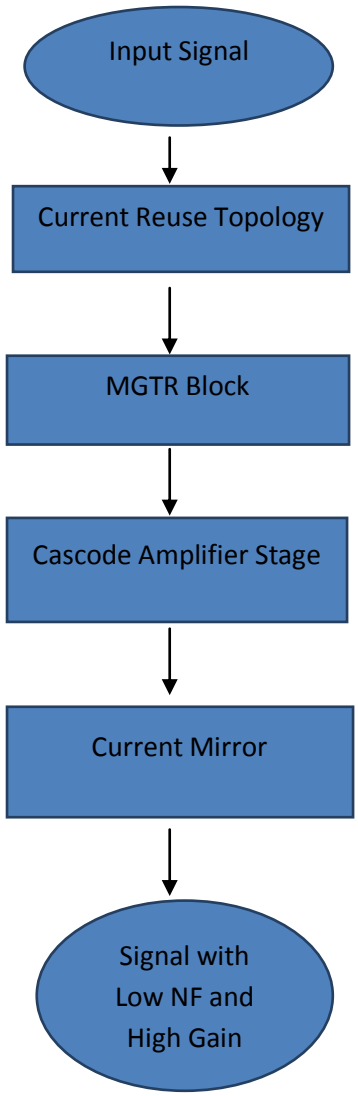


Figure 3: Flowchart of Proposed System.

In the proposed topology Input is given to current reuse block in which nBack to back inverters are connected and is use for better reception of signal for better linearity MGTR block is employed. So as to amplify cascade amplifier circuit is used at last current mirror is used for making Low Input reflection and maintaining constant current. input Is Given Differentially for better noise performance.

2. Algorithm- Get input from user with low amplitude Implementation of current reuse topology for better reception and Providing high Gain.Formation of MGTR block is used for enhancement of linearity Formation of Cascode amplifier for providing large gain Implementation of current mirror for obtaining constant current

IV. RESULT

1. Input and Output Matching

1.1 Input Matching S11

Figure 4.2 shows schematic simulated result of the input reflection coefficient (s11) and it denotes how much signal is reflected form the input port. According to IEEE standard it should be negative but it is good if its less than or equals to -10db. Its value ranges from -3dB to -4dB and minimum input reflection coefficient is obtained as -20dB @ 7.20GHz.

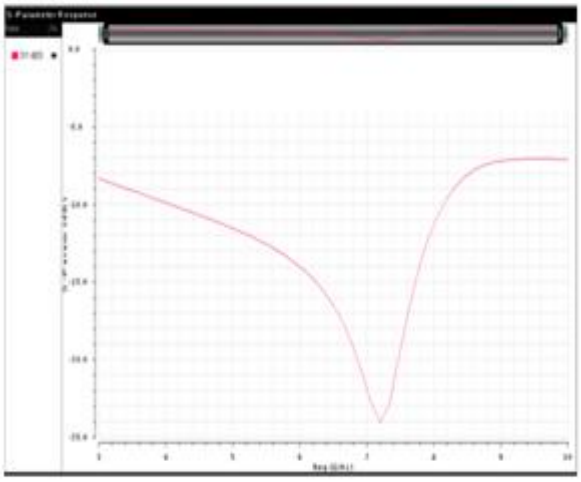


Figure 4: Input Matching Coefficient for the LNA.

Results shows that the LC ladder network at the input of LNA is best suited for purpose of input matching.
S22 Output Matching Coefficient It determines the output matching of the LNA. It also improves the output reflection coefficient, provided an enhanced gain of small signal at the output.

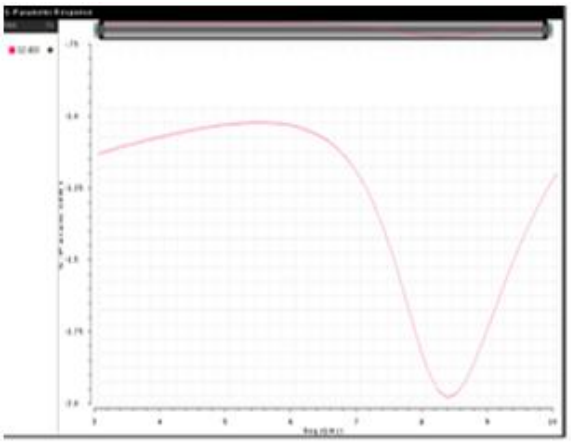


Figure 5: output reflection coefficient.

1.2 Reverse Isolation- Figure 5.4 shows simulated result of reverse isolation of LNA. According to IEEE

standard it should be < -40db in a frequency range of 3.1-10.0 GHz. It shows resistance against the unwanted signal transfer from the subsequent stages back through the LNA. These unwanted signals propagating back through the LNA could cause significant distortion. As shown in graph S12 is <-40.15dB hence it is well isolated from unwanted signals.

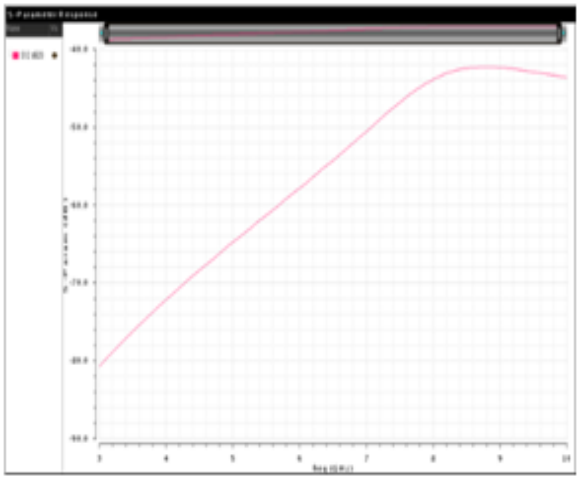


Figure 6: Reverse Isolation S12.

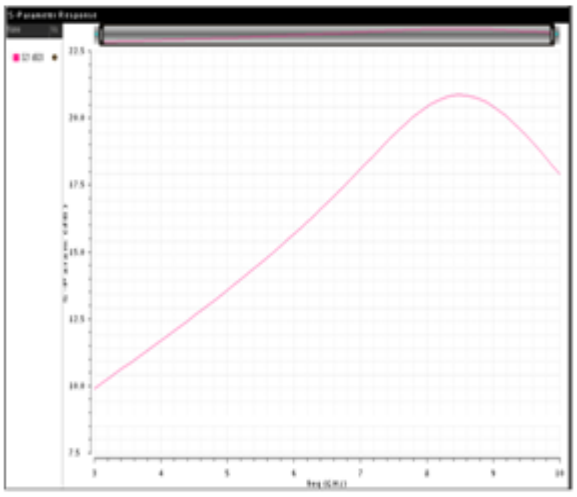


Figure 7: Gain (S21)

2. Gain

The overall gain for the proposed LNA over the entire band (3.1-10.0 GHz) is more than 10dB and the maximum gain is achieved at frequency in range of 8-9 GHz of 20.37dB. the s-parameter S21 determines the gain of the LNA.

3. 3rd order Input Intercept point

Figure 5.6 shows third order intercept point, it shows the intermodulation effect of two tone analysis at 5 and 5.1GHz. the point -3.37dBm is obtained which shows the circuit exhibit good linearity. This point should be as high as possible which directly indicates good linearity.

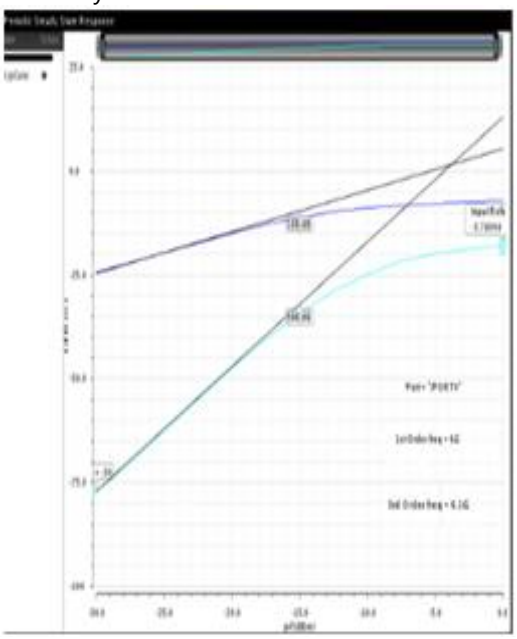


Figure 8: IIP3

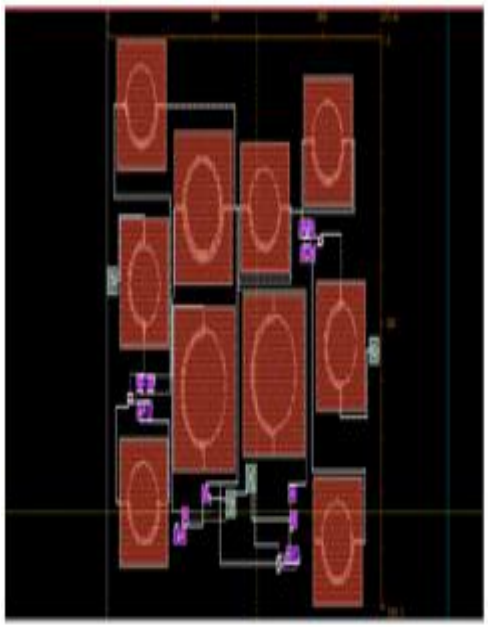
4. Layout Design

The layout of the integrated circuit that appear on the mask is used in fabrication. For designing a layout of any circuit some design rule and techniques are taken into consideration. We have used some techniques to increase the robustness and performance of the circuit.

Design rule:While the width and length of each transistor id determined by the circuit design, most of the other dimension in a layout are dictated by design rule i.e a set of rule that guarantees proper transistor and interconnect fabrication despite various tolerances in each step of design process. For designing proposed UWB LNA various precaution are taken care of, which are listed below

Minimum Width:The width of geometrics defined on a mask must exceed a minimum values imposed by both lithography and processing capabilities of the technology. In general the thicker the layer, the greater is minimum allowable width, showing that as technologies scales, the thickness must be decreased proportionally.

Minimum spacing:In Layout design different layers must be separated by a minimum spacing. In this proposed design, generally we have avoided two close parallel lines of same metals to minimize paracitics generation i.e. capacitor and resistors.



V. COMPARISON OF THE OLD AND NEW WORK

Table 5 Comparison of The Eisting work And Proposed Work

Specification	[38]	[39]	[40]	Proposed work
Technology(µm)	.18	.18	.18	.18
Frequency(GHz)	3.1 to 10.6	0.4 to 1.0	3.1 to 10.6	3.1 to 10
Input return loss(s_{11})	<-10	-12.3	<-11db	-10.5
Voltage gain(s_{21})	15.25	20.57	15	22.37
Reverse isolation (s_{12})	<-45	<-23	<-38	<-43
Output return loss(s_{22})	10			
Supply voltage	1.5	1.8	1.8	1.8
Noise figure	2.8-4.7	1.6 to 3.5	3.5 to 3.9db	1.5 to 3.507
IIP_3	-7	-3.8	6.4dbm	-3.30db @ 6 and 6.1GHz
Power dissipation(mw)	14.3	14.03	16.2	22

VI. CONCLUSION AND FUTURE WORK

Conclusion- Low Noise Amplifiers are an important component used in different RF Transceivers (Wi-Max, Wi-Fi, WLAN, WCDMA, Bluetooth etc.). They provide amplification, good matching and minimal noise to the system while maintaining linearity. Since, CMOS technology has become dominant because of its several advantages such as low cost, low static power dissipation and low area, the design of low noise amplifier using CMOS technology was top choice for design of Low Noise Amplifier.

The single ended and differential LNA was designed to operate in a WCDMA reception range using a BSIM3V2 model (Level 49) CMOS UMC 0.18µm technology in X-Circuit Open Siurce EDA Tool. The key issues in the design, gain, noise and linearity were considered. The LNA's was designed to provide high gain, matching to 50Ω RF system, good linearity and minimum noise on the operation of the circuit.

Future Scope- In future, for investigating design of Low Noise Amplifiers for RF applications following work may be extended:Since Balun is used for input output coupling and it degrades the noise figure for this Different Coupling techniques can be used for giving and taking output from the circuit such as capacitive coupling, transformer coupling etc.

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