

A Review of Reversible Logic-Based Architectures for Ultra-Low-Power CPUs

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Abstract- Energy dissipation, rather than transistor density, now limits the performance of general-purpose processors, and conventional complementary metal-oxide-semiconductor (CMOS) logic is approaching practical efficiency limits because every erased bit and every abruptly charged node releases energy as heat. Reversible computing addresses this problem by preserving information throughout a computation so that, when combined with adiabatic switching, most of the signal energy can in principle be recovered rather than dissipated. This paper presents a focused review of reversible logic-based architectures for ultra-low-power central processing units (CPUs). Literature drawn from IEEE Xplore, SpringerLink, ScienceDirect, American Physical Society and Nature Portfolio journals, and related sources is organized into four themes: thermodynamic foundations and reversible gate libraries; reversible instruction-set and processor architectures; physical implementation technologies, including adiabatic CMOS, adiabatic superconductor logic, ballistic fluxon logic and quantum-dot cellular automata; and evaluation practice. The comparative analysis shows that logically reversible processors have been specified and simulated, and that adiabatic superconductor microprocessors have been demonstrated, but no reviewed study reports measured system-level energy savings for a fully reversible CPU. Key gaps include efficient resonant power-clock generation, leakage and cryogenic overheads, garbage management and inconsistent evaluation metrics. A conceptual layered architecture is proposed to frame these challenges and guide future research.

Keywords— Reversible computing, Adiabatic logic, Landauer limit, Reversible processor architecture, Adiabatic quantum-flux-parametron, Ultra-low-power CPU

I. INTRODUCTION

For several decades, processor energy efficiency improved alongside transistor scaling. With the end of classical voltage scaling, however, energy per operation has become the principal constraint on computing, from battery-powered edge devices to data centers. Ho et al. [1] estimated that, under conventional irreversible assumptions, the energy efficiency of CMOS microprocessors can improve by only about two orders of magnitude beyond a 2023 state-of-the-art graphics processor before switching, interconnect and leakage limits bind. That estimate explicitly excludes reversible and adiabatic computing, which is why these approaches have attracted renewed attention as a path to continued efficiency gains [2].

The physical basis of this argument is Landauer's principle, which states that the logically irreversible

erasure of one bit must dissipate at least $k_B T \ln 2$ of energy into an environment at temperature T [3]:

$$E_{\text{erase}} \geq k_B T \ln 2 \approx 2.9 \times 10^{-21} \text{ J (at 300 K)} \quad (1)$$

Experiments using a colloidal particle in a double-well potential [4] and nanomagnetic memory bits [5] have confirmed that erasure dissipation approaches this bound. Bennett [6] showed that any computation can be made logically reversible by recording intermediate results and later uncomputing them, so that erasure, and hence the Landauer cost, is avoidable in principle. Logical reversibility alone does not save energy, however: the circuit must also be physically reversible, switching adiabatically so that the energy stored on signal nodes is returned to the power supply [7].

Existing surveys concentrate largely on reversible gates and synthesis algorithms [8]; less attention has

been paid to how reversibility propagates through a complete central processing unit (CPU), from instruction set and control to datapath, memory and power delivery. Its objectives are (i) to synthesize the main architectural approaches to reversible CPUs, (ii) to compare candidate implementation technologies, (iii) to identify research gaps supported by the evidence, and (iv) to propose a conceptual architecture that connects these layers.

II. REVIEW APPROACH

This is a focused narrative review rather than a systematic one. Literature was identified through IEEE Xplore, SpringerLink, ScienceDirect, APS, Nature Portfolio, IOP and IEICE journals, institutional repositories and arXiv, using terms such as “reversible processor”, “reversible ALU”, “adiabatic logic” and “adiabatic quantum-flux-parametron”. Foundational works were retained and studies from 2019–2026 prioritized. Studies were included when they addressed processor architecture, a processor datapath component, or a logic technology capable of physically reversible operation. Bibliographic details were checked against publisher pages, DOI records or institutional repositories.

III. FOUNDATIONS AND REVERSIBLE GATE LIBRARIES

1. Logical and Physical Reversibility

A logic function is logically reversible when its inputs can be reconstructed uniquely from its outputs, which requires a bijective mapping with equal numbers of inputs and outputs. Fredkin and Toffoli's conservative logic [9] showed that universal computation is possible with reversible primitives, and the Toffoli (controlled-controlled-NOT) and Fredkin (controlled-swap) gates remain standard building blocks. Peres [10] introduced a gate that combines Toffoli and controlled-NOT operations at lower cost. Physical reversibility is a separate property: the circuit state must evolve quasi-statically so that dissipation falls as the transition time increases. For adiabatic charging of a node capacitance C through a resistance R over a ramp time T , the dissipated energy is approximately [7]

$$E_{\text{diss}} \approx (RC/T) C V_{\text{DD}}^2 \quad (2)$$

which decreases as T increases, in contrast to the $\frac{1}{2}CV_{\text{DD}}^2$ lost in each conventional charging event. Logical reversibility is what allows every node to remain adiabatic: once information is erased, its stored charge cannot be recovered without an abrupt, dissipative transition [2], [11].

2. Reversible Synthesis and Gate-Level Design

Reversible circuits prohibit fan-out and feedback loops, so copying requires explicit gates, and irreversible specifications must be embedded using constant inputs (ancillae) and unused garbage outputs [8]. Saeedi and Markov [8] surveyed optimal, heuristic and post-synthesis methods; their dominant metrics, gate count and quantum cost, derive from quantum computing and do not directly measure classical energy. The recent PXG gate [12], for example, attains a quantum cost of 3 with 10 transistors in 45 nm CMOS, but it was evaluated as a static CMOS circuit with a 1 V supply, without energy recovery and through pre-layout simulation only; its 1.52 pJ power–delay product therefore reflects conventional switching losses. Reversibility at the logic level yields energy benefits only when the circuit is driven adiabatically.

IV. REVERSIBLE PROCESSOR ARCHITECTURES

1. Pendulum and Early Reversible Microprocessors

The Pendulum processor developed by Vieri [13] at the Massachusetts Institute of Technology was one of the earliest attempts to build a fully reversible microprocessor. Its instruction set was derived from a MIPS-style reduced instruction set computer (RISC) and targeted split-level charge recovery logic (SCRL). Expanding operations such as AND were XOR-accumulated into the destination register, memory used an exchange operation that swaps values rather than overwriting them, and branches exchanged the program counter with a target address while preserving the information needed for reverse execution. The work showed that register transfer and memory access are comparatively easy to make reversible, whereas instruction fetch, decode and

control flow are not. Its energy argument, however, relied on an energy-recycling power supply that was assumed rather than built.

2. Formally Reversible Instruction Sets

Axelsen, Glück and Yokoyama [14] formalized reversible machine code and an abstract processor architecture, proving that a general class of instruction sets built from reversible updates is reversible and arguing that both the control logic and every instruction must be invertible. Thomsen, Axelsen and Glück [15] then designed Bob, a purely reversible architecture whose instruction set, BobISA, is locally invertible and expressive enough to serve as a compiler target for a structured reversible language, with fully reversible control logic and address calculation. Thomsen's dissertation [16] extended this line of work to garbage-free arithmetic, a reversible arithmetic logic unit (ALU), reversible functional hardware description languages and a design flow to CMOS place-and-route, including a fabricated ALU in complementary pass-gate CMOS. Together, these studies establish that a programmable reversible CPU is architecturally feasible, but their evaluation remains at the functional or gate level, and none reports measured processor-level energy.

3. Reversible Datapaths in Emerging Nanotechnology

Quantum-dot cellular automata (QCA) have been used extensively to explore reversible datapaths. Alharbi *et al.* [17] designed a multilayer QCA ALU that is both logically and physically reversible, performing 16 operations with 1,153 cells, an area of $2.14 \mu\text{m}^2$ and an average simulated energy of 0.908 meV per operation at 1 K.

Nemattabar *et al.* [18] reported a reversible QCA ALU supporting 26 arithmetic and logical operations, evaluated by cell count, area, clock cycles, quantum cost, constant inputs and garbage outputs. Both designs are simulation-based; the former is a single-bit slice simulated at 1 K, and neither addresses instruction control or memory.

V. PHYSICAL IMPLEMENTATION TECHNOLOGIES

1. Adiabatic and Reversible CMOS

Athas *et al.* [7] established the adiabatic-switching principles behind (2) and showed that energy recovery requires slowly ramped power-clock waveforms delivered by an efficient, preferably resonant, supply. Hänninen *et al.* [11] compared irreversible and Bennett-clocked reversible versions of a 4-bit adiabatic CMOS multiplier in a $2 \mu\text{m}$ process and found, through HSPICE simulation, that the reversible version consumed nearly two orders of magnitude less power below about 1 MHz, with the advantage disappearing at approximately 20–30 MHz and diminishing further with layout parasitics. Frank *et al.* [19] proposed static two-level adiabatic logic (S2LAL), presented as the first CMOS family that is both fully static and fully adiabatic apart from leakage, using eight trapezoidal clock phases and a latency of one tick per logic stage. S2LAL is quad-rail, its efficiency is ultimately bounded by leakage, and no simulation or silicon data were reported. Room-temperature reversible CMOS therefore depends on two unresolved elements: high-quality-factor resonant clock generators and low-leakage devices.

2. Adiabatic Superconductor Logic

Adiabatic quantum-flux-parametron (AQFP) logic is powered and clocked by an alternating-current excitation. Takeuchi *et al.* [20] constructed the reversible quantum-flux-parametron (RQFP) gate from AQFP elements, and later simulations [21] showed that RQFP dissipation decreases with ramp time and falls below $k_B T \ln 2$ for rise and fall times of approximately 7 ns at 4.2 K, whereas logically or physically irreversible variants retain a dissipation floor of 3×10^{-21} J or more caused by non-adiabatic state changes. Yamae *et al.* [22] experimentally demonstrated a reversible full adder built from RQFP gates for all input combinations, and an AQFP 8-bit adder has been reported with about $24 k_B T$ of dissipation per junction [23]. The MANA microprocessor [24], a 4-bit AQFP design with more than 20,000 Josephson junctions (JJs), ran as a full processor at 100 kHz, while its datapath operated at 2.5 GHz on a separate chip, with about 1.4 zJ per

junction under a 5 GHz clock. AQFP datapaths have since extended to a 16-bit Kogge–Stone adder [25] and an 8-bit ripple-carry adder whose delay-line clocking reduces latency to about 40% of a conventional design [26]. MANA is adiabatic but not logically reversible, and its energy advantage must be weighed against the overhead of cooling to 4.2 K.

3. Ballistic and Momentum-Based Reversible Logic

Ballistic approaches avoid an external power-clock altogether. Osborn and Wustmann [27] simulated asynchronous ballistic shift registers in which moving fluxons, powered only by the input bits, elastically exchange flux with a stored bit, and they reported the first asynchronous reversible two-input gate.

Ray and Crutchfield [28] proposed a Josephson-junction bit-swap based on momentum computing that, in physically calibrated simulations, operates on nanosecond time scales with dissipation below the Landauer bound. Both approaches could remove the clock-distribution problem from reversible CPUs, but they remain at the gate level.

VI. COMPARATIVE ANALYSIS

Table I summarizes representative studies, and three patterns emerge. First, processor-level work [13]–[16] is architecturally mature but energetically unvalidated, whereas technology-level work [21], [22], [24] provides measured or simulated energy only for gates, small datapaths or a logically irreversible processor.

Second, each technology exchanges one overhead for another: adiabatic CMOS needs slow ramps and efficient resonators, AQFP needs cryogenic cooling, and QCA lacks a mature fabrication route.

Third, evaluation metrics are inconsistent; quantum cost, garbage outputs, cell count, energy per junction and power–delay product cannot be compared directly, and energy per instruction, the figure of merit that matters most for a CPU, is rarely reported.

Table 1: Comparison of Representative Studies on Reversible CPU Architectures and Technologies

Study	Objective	Technology / Method	Major Reported Findings	Limitations / Gaps
Vieri [13], 1999	Fully reversible microprocessor (Pendulum)	MIPS-style reversible ISA; SCRL adiabatic CMOS	XOR-accumulate operations, exchange memory and reversible branching shown feasible	Energy-recycling supply assumed; no measured CPU energy
Axelsen <i>et al.</i> [14], 2007	Formal reversible machine code	Abstract processor; reversible-update proofs	General class of instruction sets proven reversible	Abstract model; no circuit or energy data
Thomsen <i>et al.</i> [15], 2012	Programmable reversible processor (Bob)	Locally invertible BobISA; reversible gate-level design	Fully reversible control logic and address calculation	Gate-level design; no physical energy evaluation
Hänninen <i>et al.</i> [11], 2013	Energy recovery vs. logical reversibility	4-bit multiplier; 2 μ m adiabatic CMOS; HSPICE	Nearly 100 $\times$ lower power than irreversible mode below $\sim$ 1 MHz	Advantage vanishes near 20–30 MHz; clock cost excluded
Takeuchi <i>et al.</i> [21], 2017	Reversibility vs. dissipation	RQFP vs. irreversible AQFP gates; JSIM at 4.2 K	RQFP below $k_B T \ln 2$ for $\sim$ 7 ns ramps; irreversible floor $\geq 3 \times 10^{-21}$ J	Simulation only; slow ramps; cryogenic
Yamae <i>et al.</i> [22], 2019	Reversible arithmetic	RQFP full adder; fabricated and measured	Correct operation for all inputs; dissipation falls with frequency	Single adder; not integrated in a CPU

Study	Objective	Technology / Method	Major Reported Findings	Limitations / Gaps
Frank <i>et al.</i> [19], 2020	Fully static, fully adiabatic CMOS	S2LAL; eight-phase trapezoidal power-clocks	One tick per logic stage; no floating nodes	Quad-rail; leakage-bound; no simulation or silicon data
Ayala <i>et al.</i> [24], 2021	Adiabatic superconductor CPU (MANA)	4-bit AQFP processor; > 20,000 JJs	Full CPU at 100 kHz; datapath at 2.5 GHz; 1.4 zJ per JJ at 5 GHz	Logically irreversible; 4.2 K cooling overhead
Osborn and Wustmann [27], 2023	Clock-free reversible gates	Ballistic fluxon shift registers; simulation	First asynchronous reversible two-input gate	Gate level; no processor integration
Alharbi <i>et al.</i> [17], 2023	Reversible ALU	Multilayer QCA; QCADesigner-E	16 operations; 1,153 cells; 0.908 meV per operation (average)	Simulation at 1 K; single-bit; not fabricated
Rajput <i>et al.</i> [12], 2026	Compact reversible gate	PXG gate; 45 nm static CMOS; Cadence	Quantum cost 3; 10 transistors; PDP 1.52 pJ	No energy recovery; pre-layout simulation

VII. PROPOSED CONCEPTUAL ARCHITECTURE

Fig. 1 presents a proposed conceptual architecture for a reversible ultra-low-power CPU that draws together the reviewed approaches; it has not been implemented or validated. The toolchain layer compiles a program written in a reversible language into locally invertible machine code through garbage-free synthesis [8], [15], [16]. The logically reversible core follows the Pendulum and Bob principles [13], [15]: instructions are moved from an exchange-based instruction memory, decoded by a fetch unit that retains the current and previous program-counter values so that decoding can be undone, and executed by a register file and ALU that use swap and XOR-update operations instead of overwrites. Branch and direction control stores the information needed for reverse execution. Intermediate values are held in a history and ancilla buffer and removed by Bennett's compute-copy-uncompute schedule [6]. Unavoidable information loss, chiefly at input/output (I/O), is confined to an explicit irreversible boundary where each erased bit costs at least $kBT \ln 2$ and can be counted and minimized.

Fig. 1. Proposed conceptual architecture of a reversible ultra-low-power CPU, showing the

toolchain, logically reversible core, irreversible boundary and physical power-clock layer (synthesized from [7], [13], [15], [19], [24]; not an implemented system).

The physical layer supplies multiphase power-clock signals from a resonant LC or microelectromechanical (MEMS) generator and returns recovered charge to it [7], [19]. The core can be mapped onto adiabatic CMOS for room-temperature operation or onto AQFP/RQFP logic for cryogenic systems [21], [24]. An energy and timing monitor feeds measured dissipation and error rates back to the clock generator so that the ramp time T in (2) can be adjusted at run time, trading speed for energy; this feedback loop has not been demonstrated in the reviewed literature.

VIII. RESEARCH GAPS AND FUTURE DIRECTIONS

1. Gaps Supported by the Reviewed Evidence

- System-level validation: No reviewed study reports measured wall-plug energy per instruction for a logically reversible CPU. Pendulum assumed its recycling supply [13], Bob and its successors were evaluated at gate level [15], [16], and S2LAL has no published silicon data [19].

- Power-clock efficiency: Energy recovery in CMOS depends on resonant clock generators whose losses can offset logic-level savings, and their cost has not been quantified at processor scale [7], [11].
- Leakage and frequency limits: The benefit of reversible adiabatic CMOS disappears above tens of megahertz in older processes [11] and is ultimately bounded by leakage [19].
- Cryogenic overhead: AQFP offers zeptojoule-scale switching, but cooling overhead and low full-system test frequencies limit processor demonstrations [24], [25].
- Garbage and memory overhead: Reversible instruction sets must store or uncompute history, which increases state and latency [8], [14].
- Evaluation metrics: Inconsistent figures of merit prevent fair comparison across technologies [8], [12], [17].

2. Future Directions

Directions that still require investigation include hybrid CPUs that partition reversible datapaths from irreversible control and I/O with explicit accounting of erasure at the boundary; co-design of reversible instruction sets with garbage-aware compilers; high-quality-factor on-chip or MEMS resonators integrated with adiabatic CMOS; reversible AQFP processors that extend MANA-class designs with RQFP datapaths; asynchronous ballistic logic for clock-free cores [27]; and a shared benchmark suite that reports energy per instruction, including clock-generation and cooling overheads.

IX. CONCLUSION

This review examined reversible logic-based architectures for ultra-low-power CPUs, from thermodynamic foundations through instruction-set design to physical implementation. The literature shows that reversible processors are architecturally feasible, that reversible instruction sets can be formally specified and targeted by compilers, and that simulations of reversible superconductor gates indicate dissipation below $kBT \ln 2$. It also shows that logical reversibility yields energy benefits only when paired with physically adiabatic operation and

efficient energy recovery, and that no fully reversible CPU has yet been demonstrated with measured system-level savings. Closing this gap will require co-design across the toolchain, architecture, circuit and power-delivery layers, together with consistent evaluation metrics, for which the proposed conceptual architecture offers one framework.

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