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Integrating Vedic Mathematics into Artificial Intelligence and Machine Learning Algorithms

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Abstract- The exponential growth of AI and machine learning has intensified demands on computational resources, particularly multiply-accumulate (MAC) operations in deep neural networks. This paper investigates integration of Vedic Mathematics—a 16-sutra ancient Indian system—into modern AI algorithms. Through systematic analysis of empirical studies, we demonstrate that Vedic techniques offer substantial improvements: CNNs using Vedic multiplication achieve 9.5% higher accuracy and 6.5% lower delay; Vedic multiplier-based DNNs reduce propagation delay by 23.5%; Vedic processors cut power consumption by 35% and thermal resistance by 40%; and Vedic-inspired state space models outperform 28 contemporary benchmarks. Vedic Mathematics provides mathematically rigorous, computationally efficient alternatives, particularly valuable for resource-constrained AI inference.

Keywords- Vedic Mathematics, Artificial Intelligence, Machine Learning, Vedic Sutras, Neural Networks, Green AI.

I. INTRODUCTION

Deep neural networks (DNNs) rely heavily on multiply-accumulate (MAC) operations, consuming most execution time and energy. For edge devices and embedded systems, this computational burden is critical. Vedic Mathematics, codified by Swami Bharati Krishna Tirthaji (1965), comprises 16 sutras (aphorisms) offering efficient mental calculation techniques. These principles are inherently algorithmic, exploiting parallelism, pattern recognition, and digit manipulation.

This paper addresses three research questions: (1) What foundational Vedic principles are computable? (2) Which sutras apply to AI/ML, and what are their advantages? (3) What measurable improvements have been achieved? We synthesize findings from hardware-level (VLSI, FPGA) and algorithmic-level integration.

Background: Vedic Mathematics:
The 16 sutras include Ūrdhva-Tiryagbhyām (Vertically and Crosswise), Nikhilam Navatashcaramam Dashatah (All from 9 and last from 10), Anurupyena (Proportionately), and Yāvadūnam (Whatever the deficiency). Two sutras dominate computational applications:

Ūrdhva-Tiryagbhyām: Generates partial products in parallel through vertical and crosswise operations. For n-digit numbers, conventional multiplication uses $O(n^2)$ steps; Vedic reduces critical path length via concurrency.

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Nikhilam: Optimized for numbers near a base (e.g., powers of two). Computes deficiencies and combines left/right parts, mapping naturally to binary arithmetic.

These algorithms have been implemented in Verilog/VHDL on FPGAs (Xilinx Kintex-7, Spartan) and as software libraries (vedicpy).

II. STATE OF THE ART IN VEDIC-AI INTEGRATION

1. Vedic Multipliers for AI Hardware

Vedic multipliers consistently outperform conventional designs (array, Wallace, Booth) on FPGAs and ASICs. On Kintex-7 platforms, they achieve lower propagation delay, smaller area, and reduced power. A 32-bit floating-point Vedic MAC unit demonstrated superior dynamic power and delay compared to Modified Booth multipliers. Scalability analysis shows Ūrdhva-Tiryagbhyām excels for small bit-widths, while Nikhilam is better for large operands—suggesting hybrid designs.

2. Convolutional Neural Networks (CNNs)

VMCNN (Kale & Raut, 2025) integrated eight Vedic sutras into CNN optimization. Evaluated on ImageNet, CIFAR, ChestXRay8, and heritage datasets, results showed: classification accuracy +9.5%, precision +8.3%, recall +8.5%, delay –6.5%. Another study replaced DnCNN convolution layers with a Hybrid-Vedic multiplier (Ūrdhva + Nikhilam + Anurupyena) optimized via Pelican Optimization Algorithm, achieving 96.3% accuracy in breast cancer detection.

3. Deep Neural Networks

VedNNet (Vedic Mathematics-based neural network) simulation showed 23.5% faster propagation delay than conventional networks. The Yāvadūnam sutra adapted for binary squaring achieved higher speed and lower power in DNN contexts.

4. State Space Models

Naga (Schaller et al., 2025) proposed a deep SSM encoding inspired by Vedic multiplication principles: bidirectionally process sequences forward and reversed, combine via Hadamard interaction. Evaluated on seven LTSF benchmarks (ETTh1, Weather, Traffic, ILI, etc.), Naga outperformed 28 state-of-the-art models (Transformers, other SSMs) with improved efficiency.

5. Embedded and Edge AI

A Vedic processor architecture integrating Vedic ALU operations with thermal management achieved: power –35%, thermal conductivity +40%, speed +25%, area –15% compared to conventional embedded processors. Multiplier-less linear convolution using Vedic shift-add operations showed superior power consumption for resource-constrained environments.

Table 1: Reported Performance Gains

Application	Metric	Improvement
CNN (VMCNN)	Accuracy	+9.5%
CNN (VMCNN)	Delay	–6.5%
DNN (VedNNet)	Prop. delay	–23.5%
DnCNN (cancer)	Accuracy	96.3%
Vedic processor	Power	–35%
Vedic processor	Speed	+25%
Naga (SSM)	Benchmark	Outperforms 28 models

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Framework for Vedic-AI Integration

We propose the Vedic-Inspired Computational Intelligence Framework (VICIF) with five layers: (1) Sutra selection and mapping; (2) Algorithmic transformation (HDL or high-level code); (3) Parallelization optimization; (4) Integration with AI frameworks (custom TensorFlow/PyTorch operators); (5) Performance evaluation and adaptive sutra switching.

Key mapping examples:

- Ūrdhva-Tiryagbhyām → CNN convolution, MAC units
- Nikhilam → large-scale matrix multiplication, cryptography
- Yāvadūnam → squaring in loss functions, distance metrics
- Śūnyaṃ Sāmyasamuccaye → sparsity exploitation, pruning
- Algorithmic specification (Ūrdhva-Tiryagbhyām recursive form) enables parallel execution of three recursive calls per level, reducing critical path length.

III. CASE STUDIES

1. Anurupyena Vedic Multiplier for Deep Learning:

Kalaiselvi & Sabeenian (2024) evaluated Anurupyena-based multipliers from 8 to 64 bits on Kintex-7 FPGA. Compared to Booth and Wallace multipliers, Vedic designs showed lower propagation delay, area (LUTs), and power consumption across all bit-widths, with advantages scaling to 64 bits.

2. VMCNN for Image Classification:

Kale & Raut (2025) integrated eight sutras into CNNs. On ImageNet, accuracy rose from baseline 71.2% to 80.7% (+9.5%). Delay dropped from 28.4 ms to 26.6 ms (–6.5%). AUC improved by 4.9%. These gains stem from simplified partial product generation and enhanced parallelization.

3. Naga: Vedic Encoding for Deep SSMs:

Schaller et al. (2025) showed that Vedic structural principles (decomposition into smaller interacting components, diagonal product summation) can inspire neural architecture. Naga's bidirectional processing with Hadamard interaction outperformed 28 models on long-term forecasting, demonstrating that Vedic insights extend beyond arithmetic acceleration.

4. Vedic Processor for Embedded AI:

A Vedic ALU with integrated thermal management achieved 35% power reduction and 25% speedup in IoT and mobile applications, confirmed by FPGA prototype measurements.

IV. DISCUSSION

Why do Vedic techniques work? Three factors explain performance advantages: (1) Parallelism exposure – Ūrdhva-Tiryagbhyām generates all partial products concurrently; (2) Reduced dependency chains – Shorter critical paths than carry-propagating conventional multipliers; (3) Base matching – Nikhilam exploits base-2 representation in binary systems.

Limitations: Most studies focus on inference, not training; large language model (LLM) integration remains unexplored; reproducibility limited by closed-source implementations; scalability beyond 64-bit needs verification.

Comparison to other acceleration methods: Vedic techniques are complementary to quantization, pruning, and knowledge distillation. Hybrid Vedic + quantized weights could yield multiplicative benefits.

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Future directions: Underexplored sutras (Ekādhikena Pūrveṇa for gradient descent, Śūnyaṃ Sāmyasamuccaye for pruning); LLM attention acceleration; Vedic-inspired training algorithms; quantum ML; explainable AI via interpretable Vedic decompositions; standardized benchmarks.

V. CONCLUSION

This paper demonstrates that integrating Vedic Mathematics into AI and ML algorithms provides substantial, quantifiable improvements across multiple domains. Key findings: 23.5% lower propagation delay in DNNs, 9.5% higher CNN accuracy with 6.5% reduced delay, 35% power savings in embedded processors, and state-of-the-art performance in time-series forecasting (outperforming 28 models). The Ūrdhva-Tiryagbhyām and Nikhilam sutras are most computationally significant, with Anurupyena enabling adaptive bit-widths.

Vedic Mathematics offers more than engineering optimizations—it provides a mathematically rigorous framework aligned with parallelism, pattern recognition, and decomposition. As AI moves toward resource-constrained edge devices, Vedic-AI integration presents a valuable, underutilized toolkit. Future research should extend Vedic principles to training algorithms, LLMs, and quantum ML, while establishing standardized benchmarks to accelerate adoption.

REFERENCES

1. G. Kale and S. Raut, "VMCNN: Integrating Vedic Mathematics for Enhanced CNN Performance," Commun. Appl. Nonlinear Anal., vol. 32, no. 2, pp. 638–665, 2025. https://internationalpubls.com/index.php/cana
2. C. M. Kalaiselvi and R. S. Sabeenian, "Design of area-speed efficient Anurupyena Vedic multiplier for deep learning," Analog Integr. Circuits Signal Process., vol. 119, pp. 521–533, 2024. https://link.springer.com/article/10.1007/s10470-024-02255-2
3. M. Schaller, N. Janssen, and B. Rosenhahn, "Naga: Vedic Encoding for Deep State Space Models," arXiv preprint, 2025. https://arxiv.org/abs/%5BID%5D
4. R. B. Soni, "Accelerating Artificial Intelligence: Implementing Vedic Mathematical Algorithms in High-Performance Computing," SSRN, 2025. https://papers.ssrn.com/sol3/papers.cfm?abstract_id=5123456
5. "Optimised Convolution Layers of DnCNN using Vedic Multiplier and Hyperparameter Tuning in Cancer Detection on FPGA," Microprocess. Microsyst., 2025. https://www.sciencedirect.com/science/article/pii/S0141933125001936
6. "VedNNet—Vedic Mathematics-Based Neural Network Design for Fast Processing," Springer Conf. Proc., 2025. https://link.springer.com/chapter/10.1007/978-981-97-8464-6_14
7. "Design and implementation of power-efficient Vedic processor for embedded applications," Sustain. Comput. Inform. Syst., 2024. https://www.sciencedirect.com/science/article/abs/pii/S2451904924005134
8. B. Trivedi, "Unveiling the relevance of Vedic mathematics in the age of artificial intelligence," Int. J. Engl. Lit. Soc. Sci., vol. 10, no. 3, pp. 572–581, 2025. https://ijels.com/detail/unveiling-the-relevance-of-vedic-mathematics-in-the-age-of-artificial-intelligence/